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MS-7817 *mATX*

Ver: 10

Intel Sharkbay platform H81

CPU:

INTEL-Haswell LGA1150

System Chipset:

INTEL-LYNX

Memory:

DDRIII (1333/1666MHz) * 2 (Dual Channel)

PWM:

VRD12 - ISL95812

OnBoard Chipset:

HD Audio Codec:RTL892

LAN-realtek8111G

SIO:NUVOTON 5533D

SPI ROM: 64 MB

Other:

DVI*1

VGA*1

SATA2*2

SATA3*2

FRONT USB2.0 *2

REAL USB2.0 *4

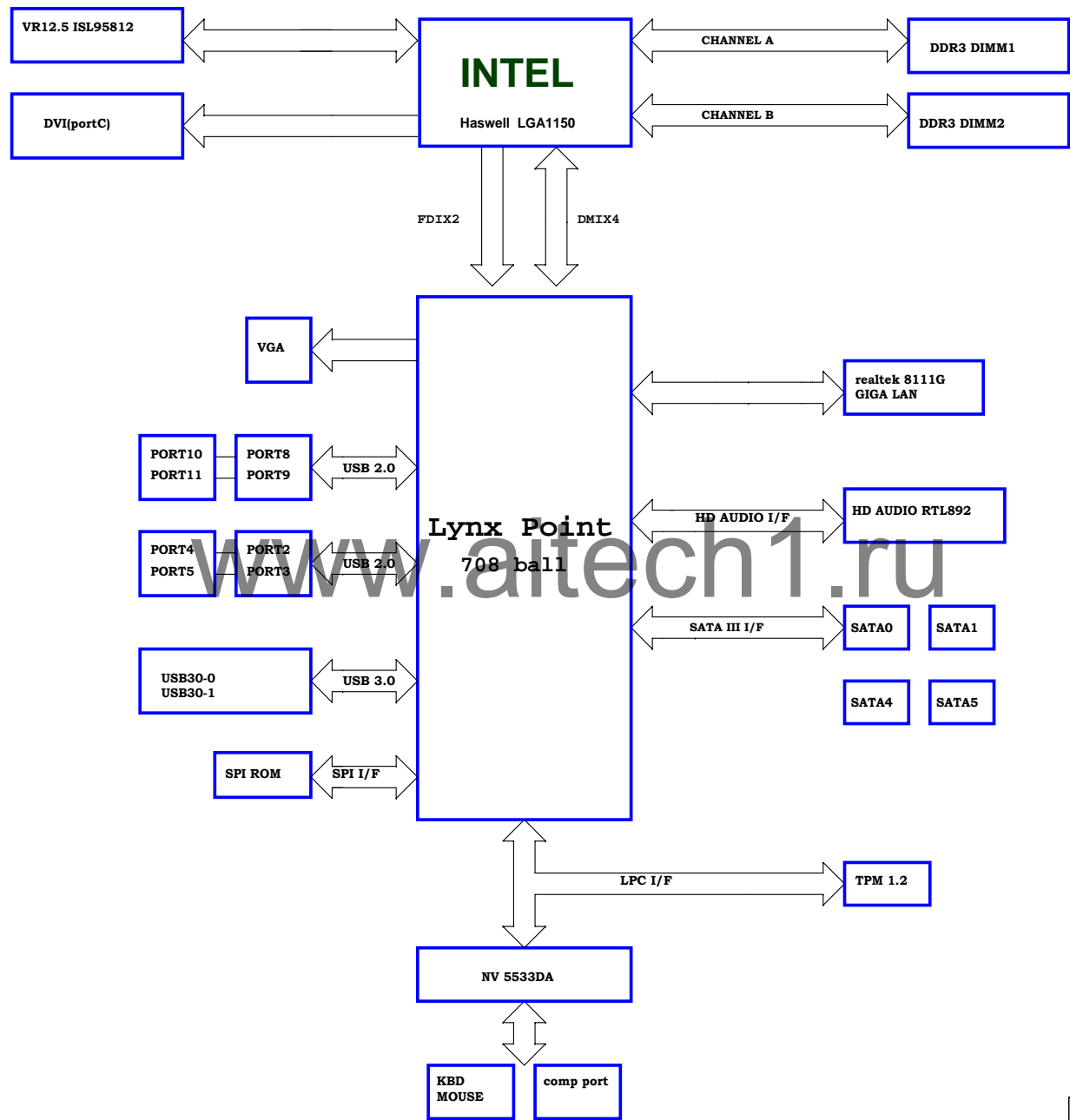
REAL USB3.0 *2

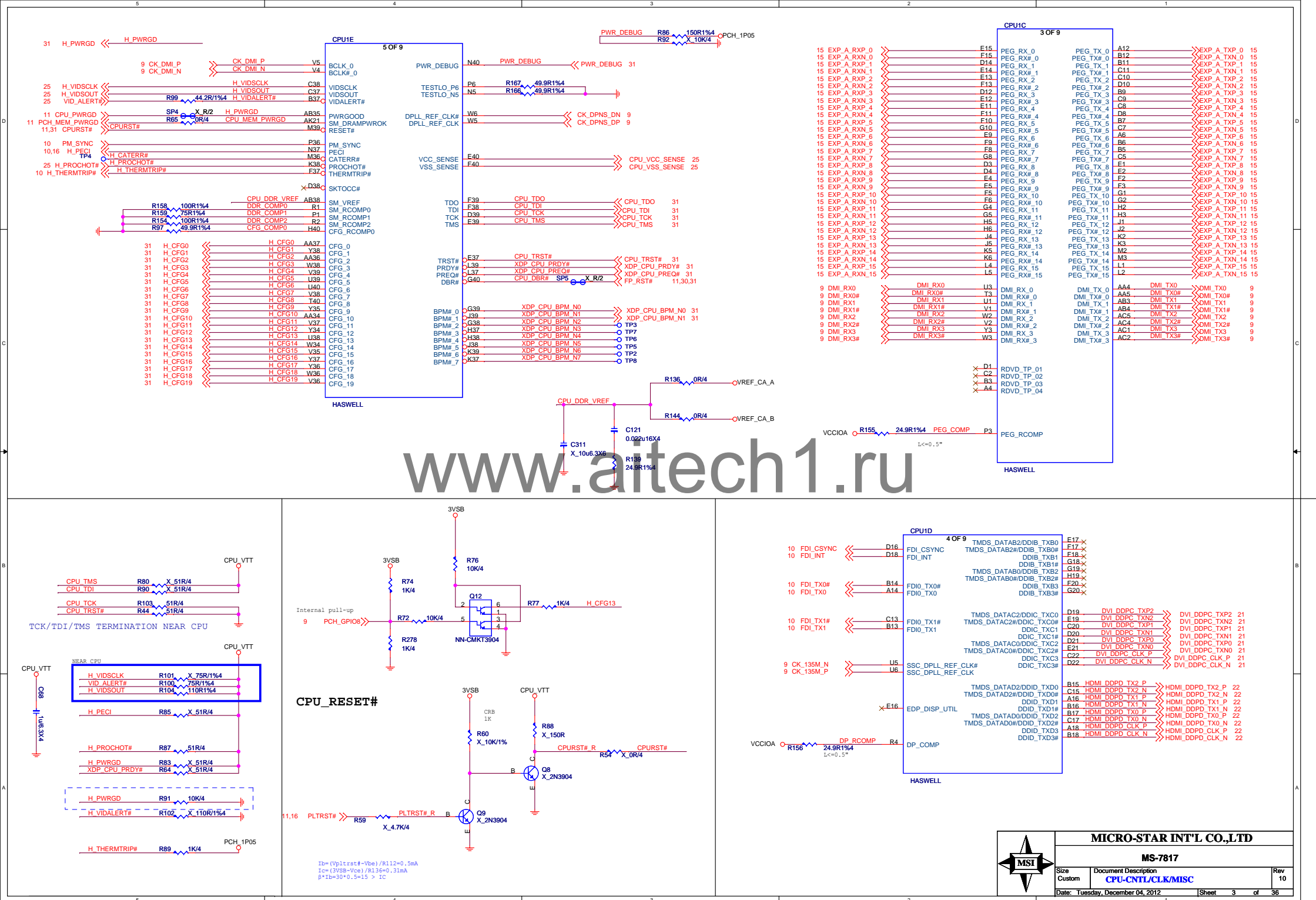
Expansion Slots:

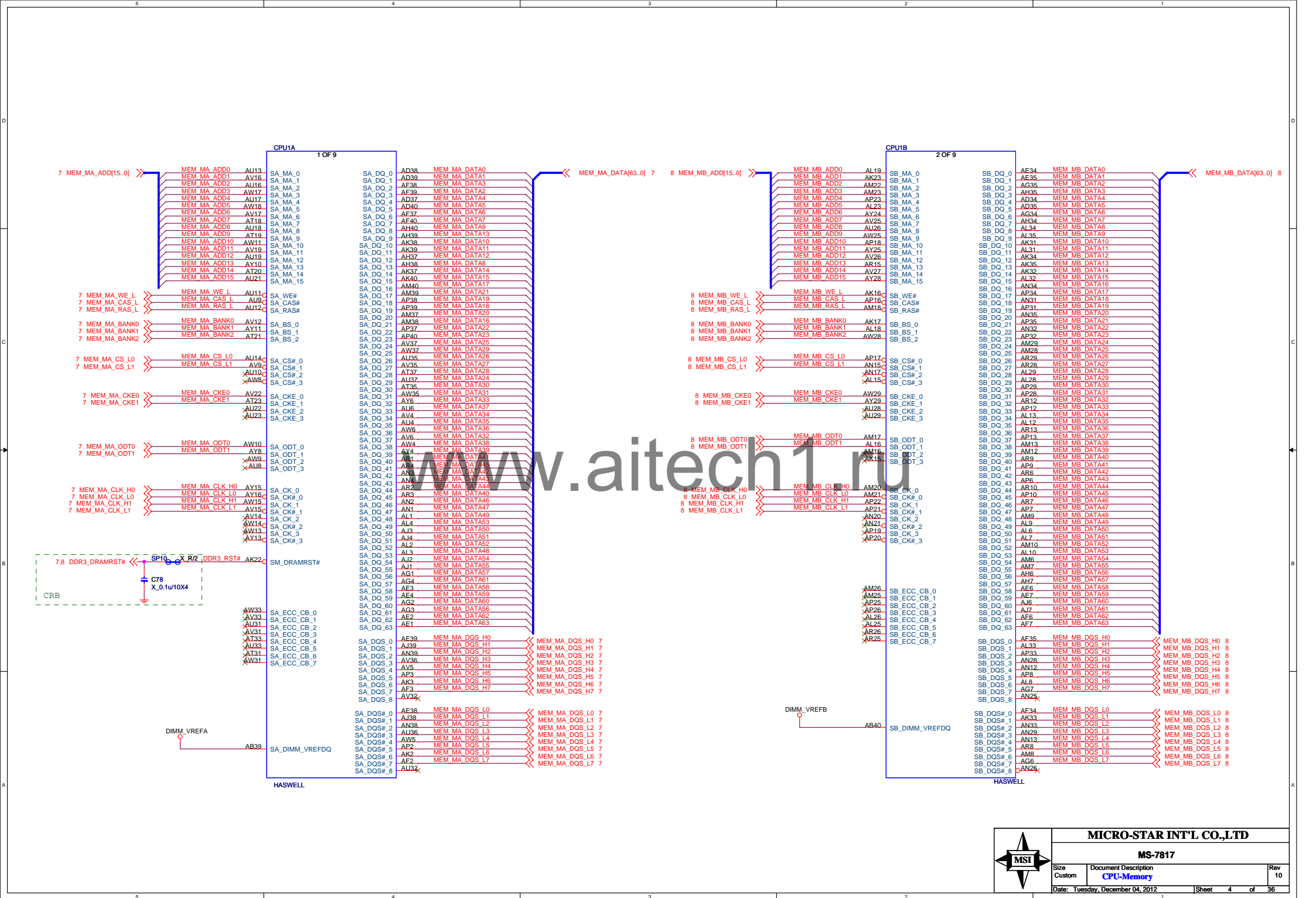
PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 1

MS-7817 Block Diagram



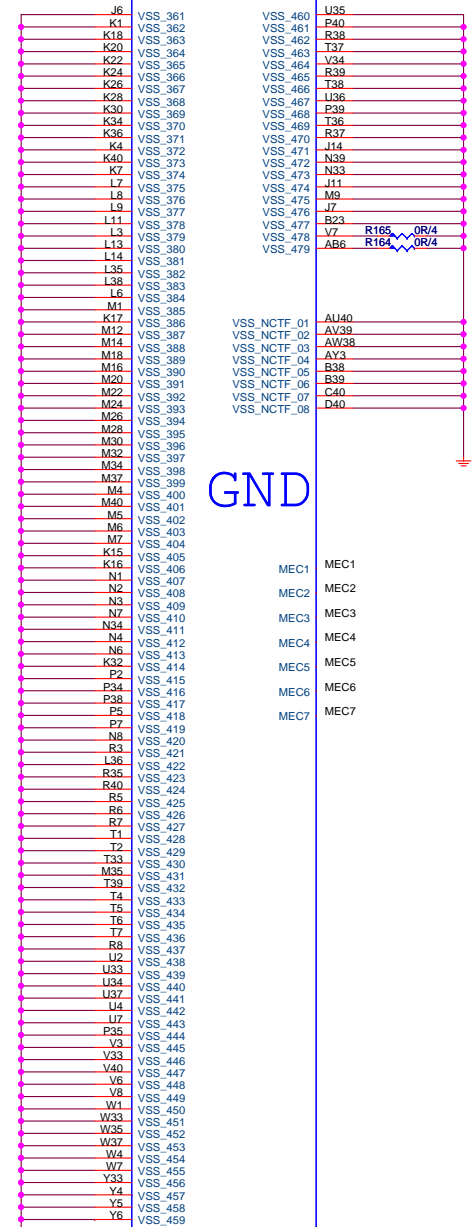




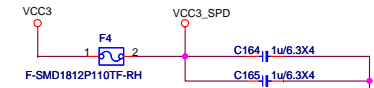
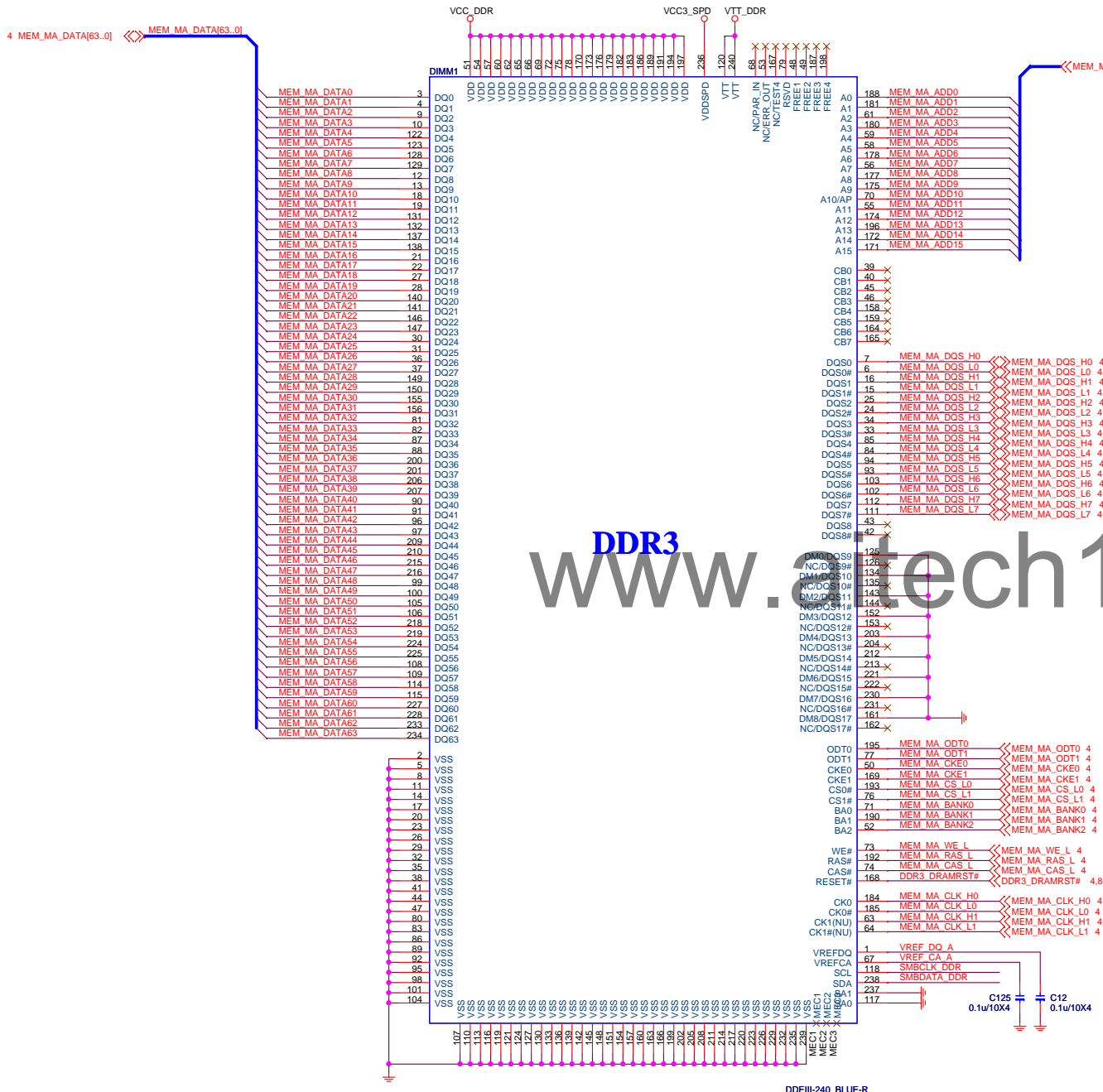
GND

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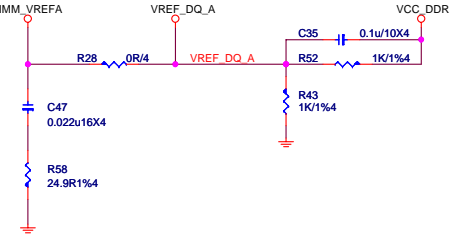
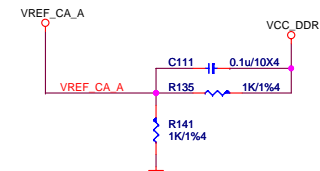
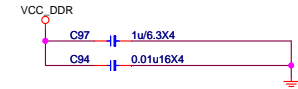
CPU1H
8 OF 9



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Place close to DIMM1



8 SMBCLK_DDR >> SMBCLK_DDR R175 33R/4 >> SMBCLK_VCC 11.27.31

8 SMBDATA_DDR >> SMBDATA_DDR R176 33R/4 >> SMBDATA_VCC 11.27.31

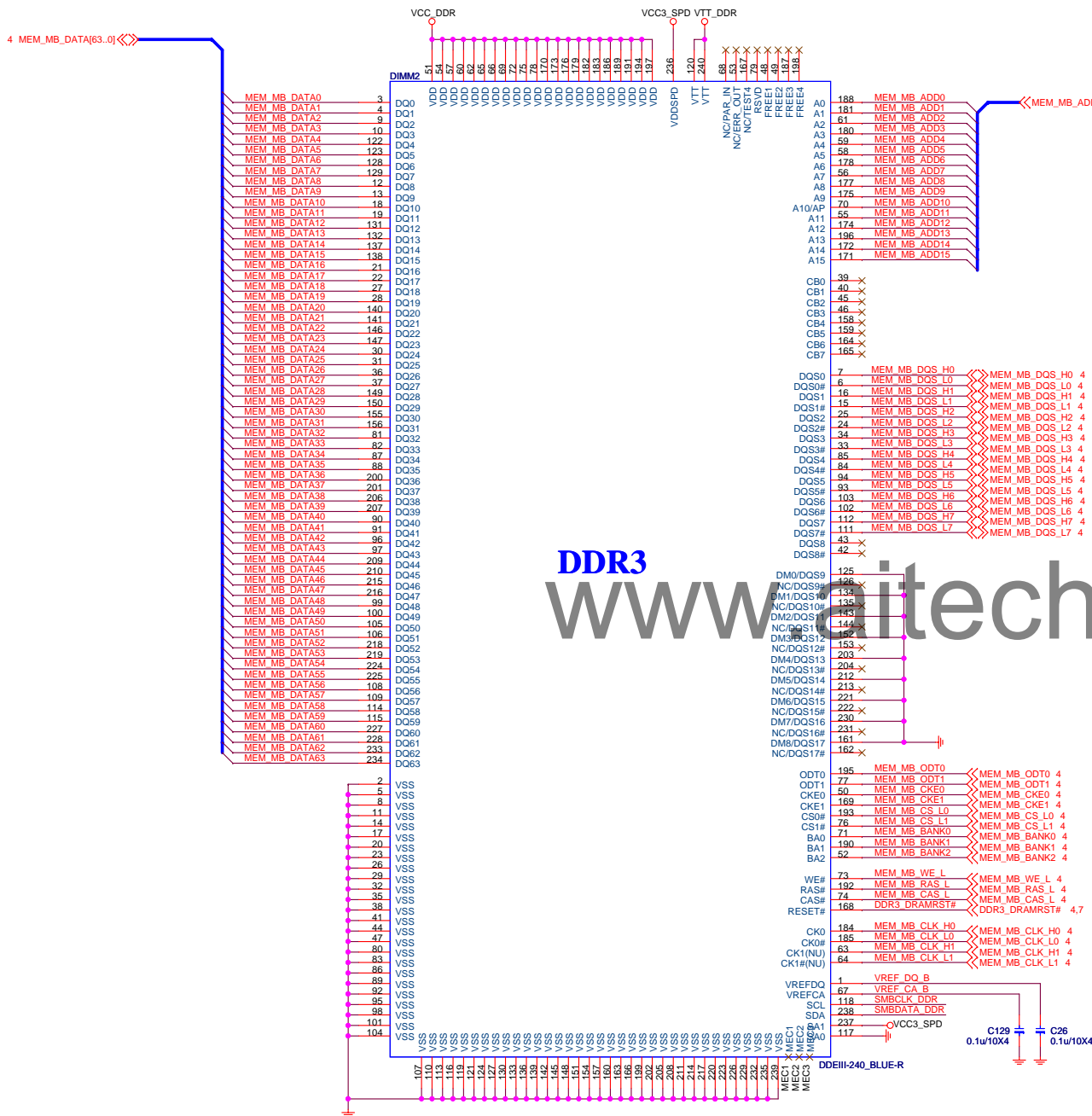
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MS-7817

Size Custom Document Description **DDR3 Chane-A DIMM1/2** Rev 10

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DDR3 DIMM_B0



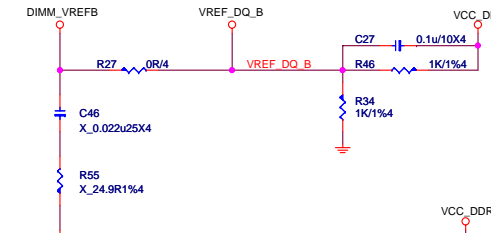
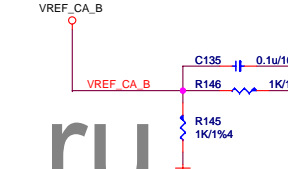
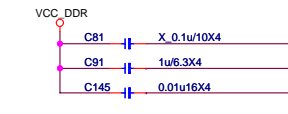
DDR3

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Place close to DIMM2

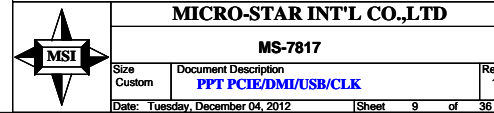
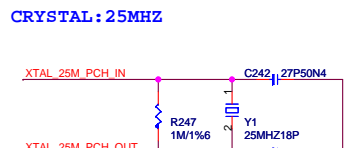
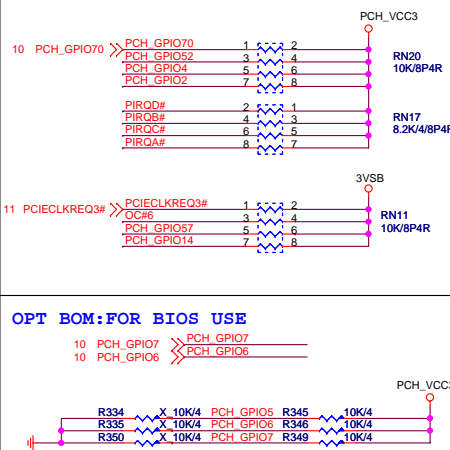
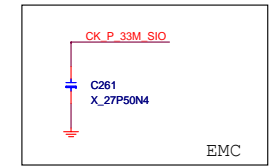


Place close to DIMM2

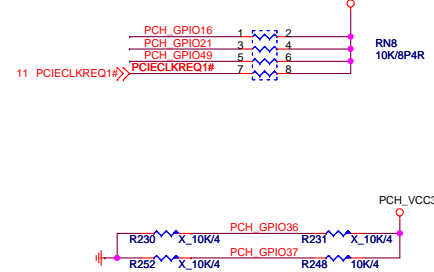
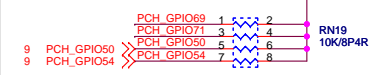


SMBCLK_DDR << SMBCLK_DDR 7
SMBDATA_DDR << SMBDATA_DDR 7

```
pcie port7,8 NA
```



SATA 6 Gb/s support on ports 0 and 1 only.



PCH_VCC3

Signal	Resistor	Delay
RGB DDC DATA	R408	2.2K/4
RGB DDC CLK	R409	2.2K/4
HDMI DDPD CTRLCLK	R401	2.2K/4
HDMI DDPD CTRLDATA	R400	2.2K/4
DVI DDPD CTRLCLK	R300	2.2K/4
DVI DDPD CTRLDATA	R306	2.2K/4

VGA R	R273	150R1%4
VGA G	R281	150R1%4
VGA B	R265	150R1%4

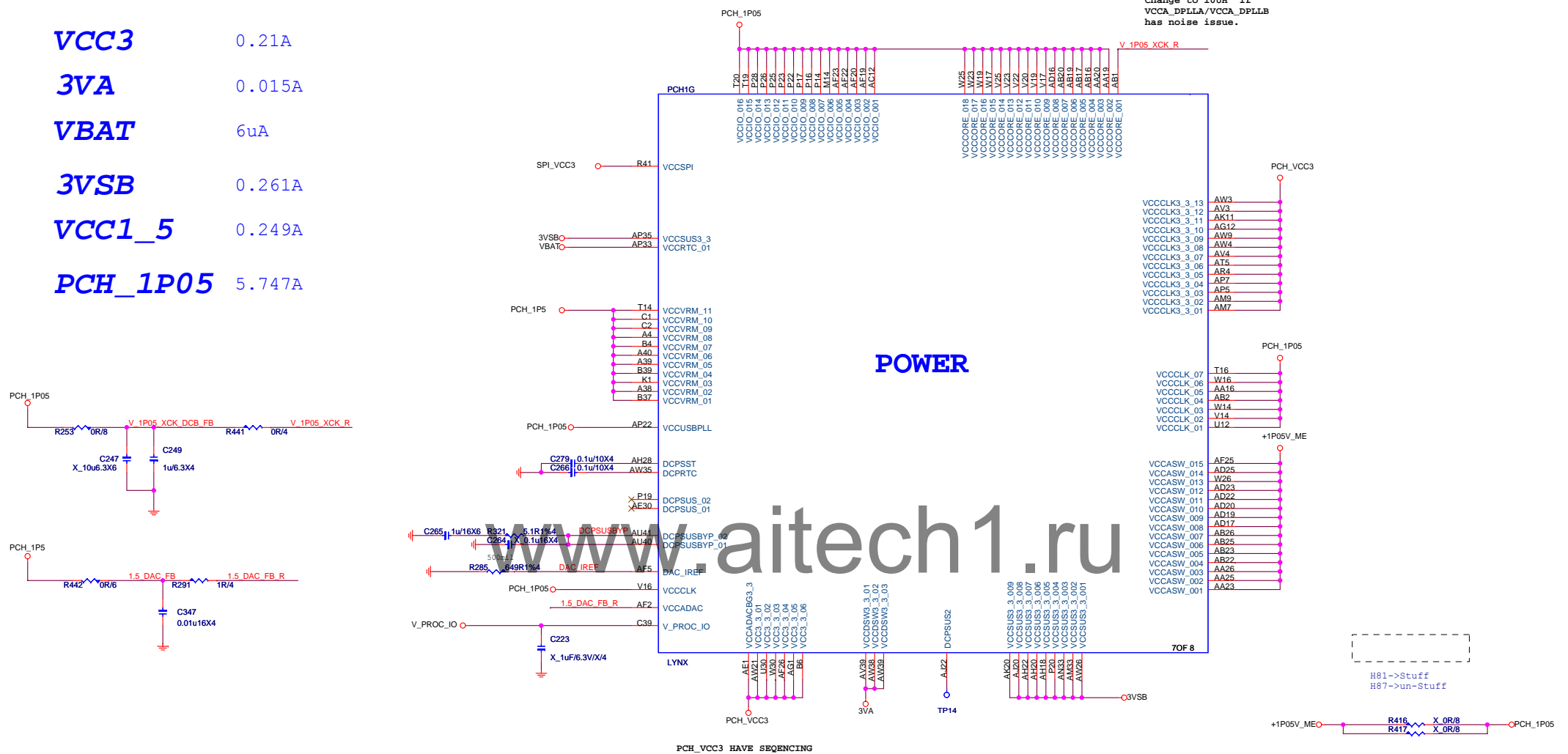


MS-7817

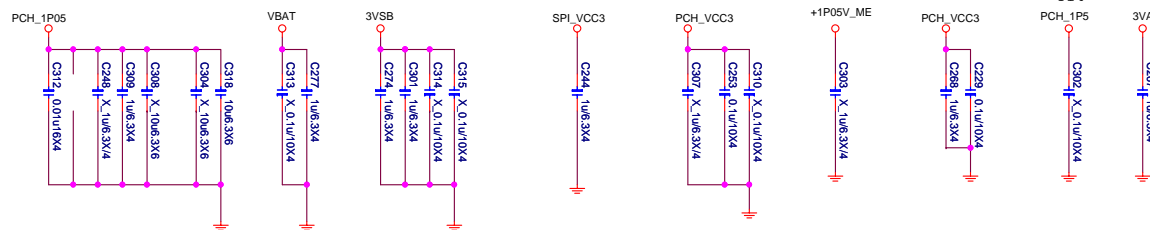
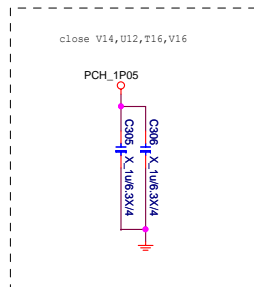
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<i>VCC3</i>	0.21A
<i>3VA</i>	0.015A
<i>VBAT</i>	6uA
<i>3VSB</i>	0.261A
<i>VCC1_5</i>	0.249A
<i>PCH_1P05</i>	5.747A



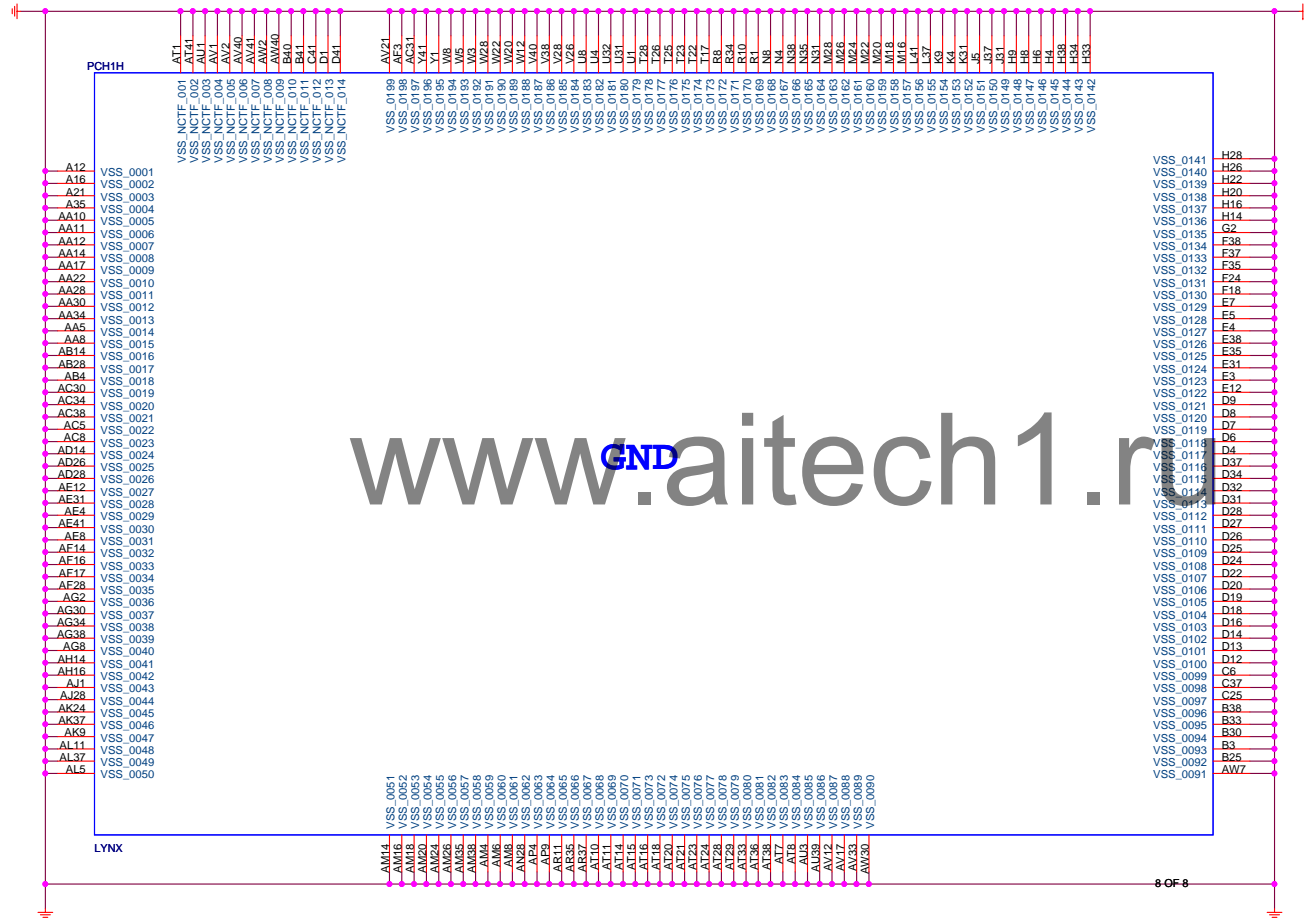
PCH decoupling cap



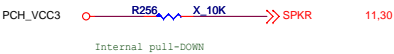
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PCH Straps

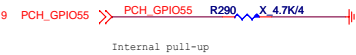


SPKR

Default Mode:

Internal weak Pull-down.

No Reboot Mode with TCO Disabled:
Connect to Vcc3_3 with 8.2k-10k Ohm weak pullup resistor.

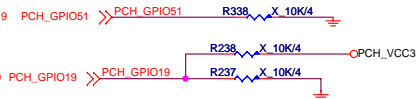


GPIO55

Default Mode:

Internal pull-up.

Top Block Swap Mode:
Connect to ground with 4.7k Ohm weak pulldown resistor.



SATA1GF/GPIO19, GPIO51

Default (SPI):

Left both SATA1GF/GPIO19 and GPIO51 floating.
No pull up required.

Boot from PCI:

Connect SATA1GF/GPIO19 to ground with 1k Ohm pull-down resistor.
Leave GPIO51 Floating.

Boot from LPC:

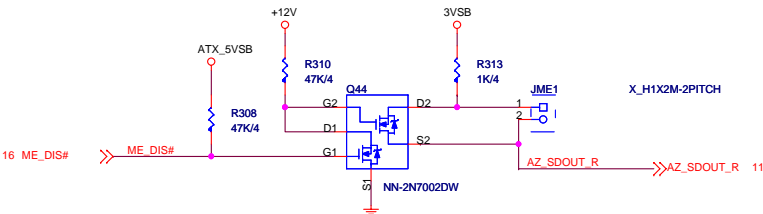
Connect both SATA1GF/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.



GPIO53

Do not pull low.

Connect to ground with 1k Ohm pull-down resistor.



HDA_SDO

Default:

Do not pull high.

Disable ME in Manufacturing Mode:
Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.

GPIO37

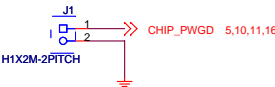
Enable TLS:

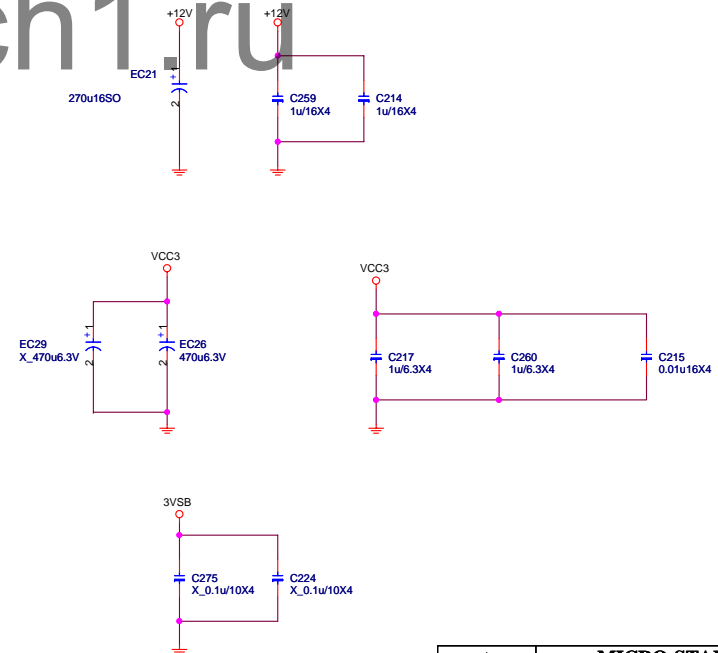
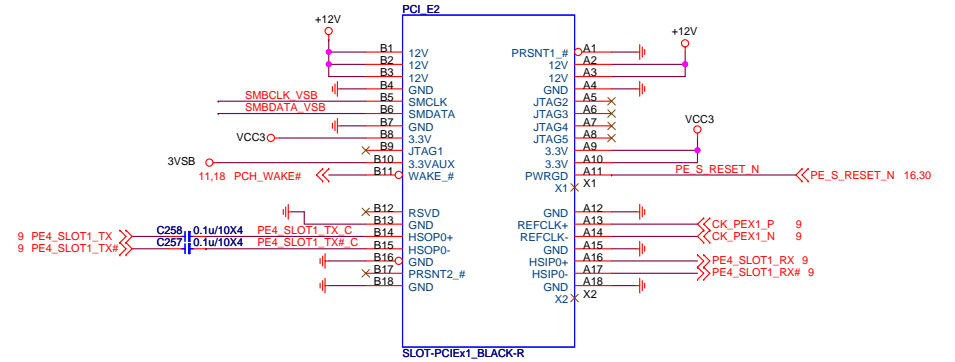
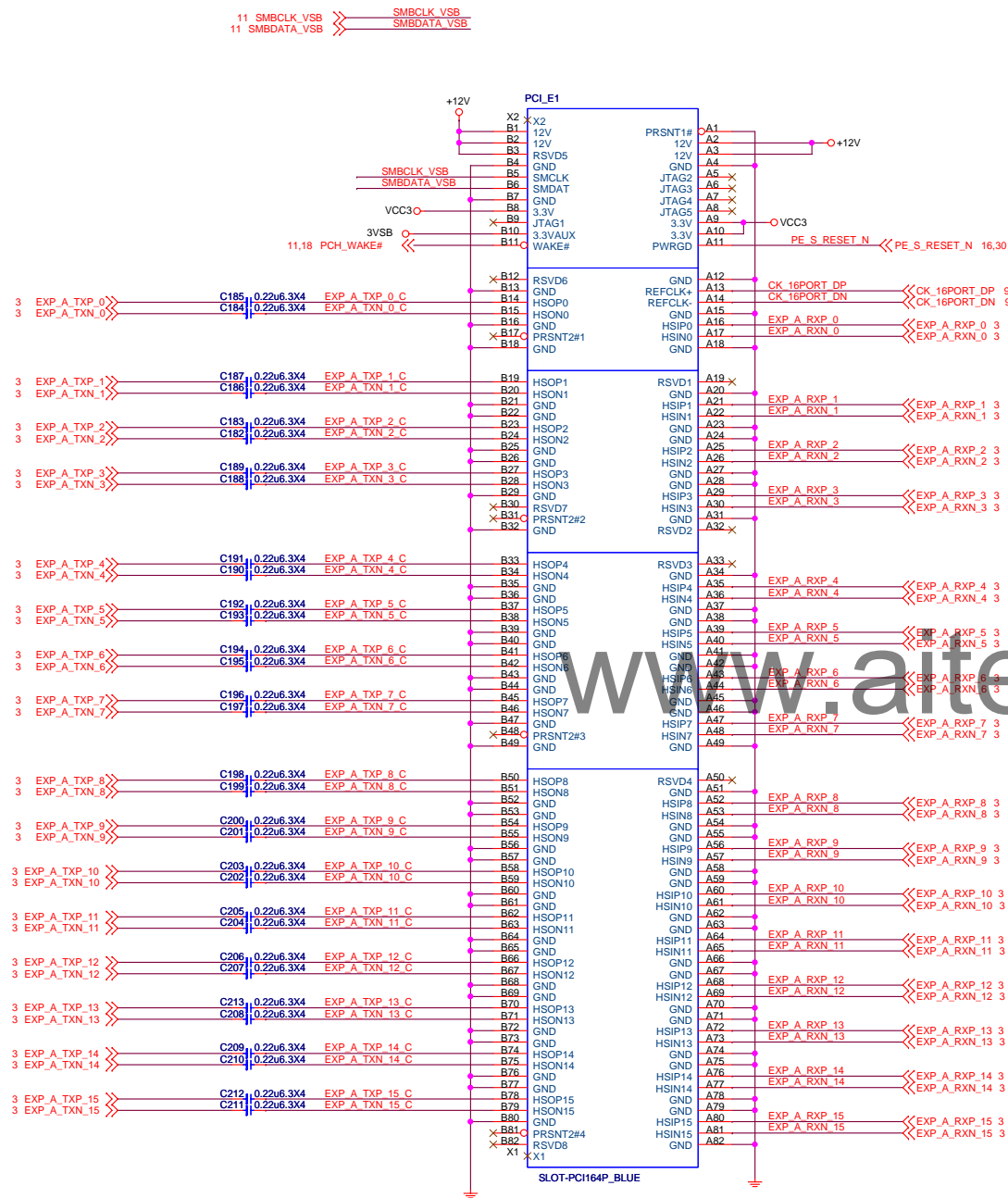
Pull up with 1k Ohm to VccSus3.3.

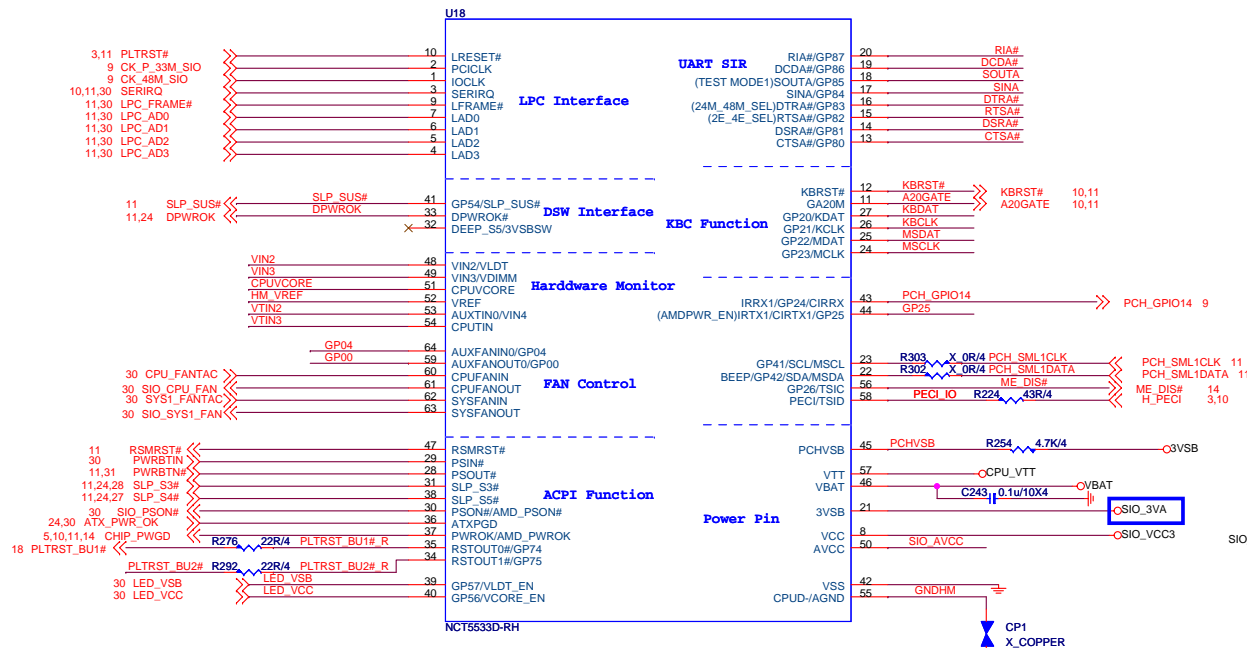
Default (Disable TLS):

Leave NC. Internal pull down.

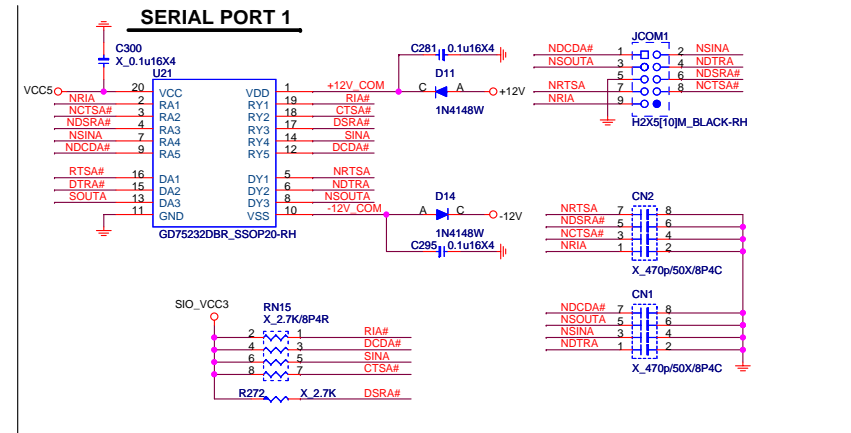
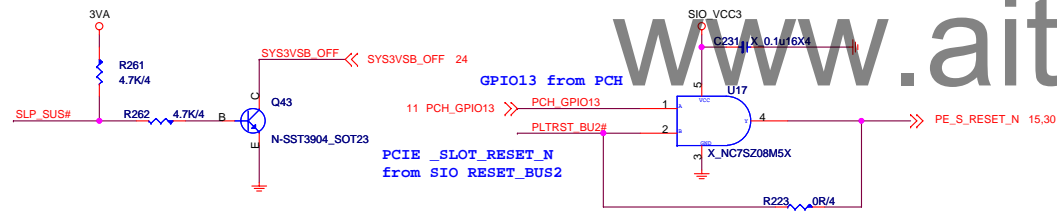
For test cpu voltage



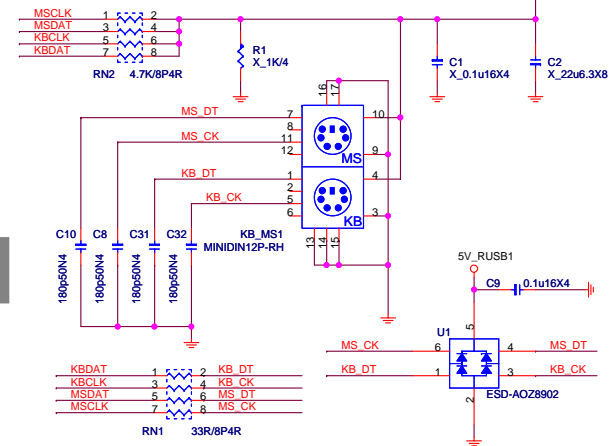




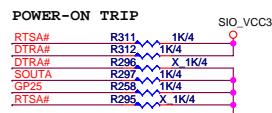
5533D DSW SUPPORT



PS2 Connector



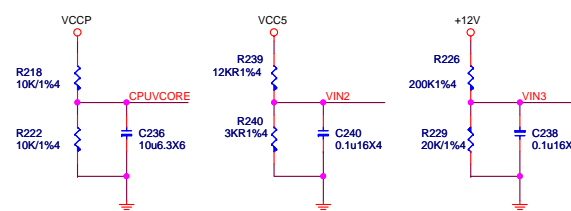
LPC I/O STRAPPING RESISTOR



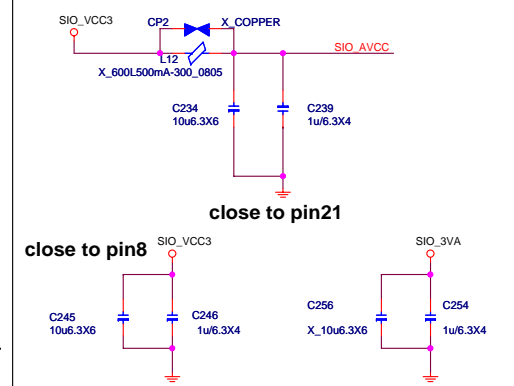
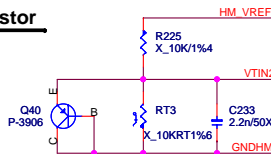
NCT5533D POWER ON STRAPPING PIN

PIN	Function	NET Name	HI	I/O
44	AMD_PWR_EN		ENABLE AMD PWR SEQ	DISABLE AMD PWR SEQ
18	TEST_MODEL1	SOUTA	TEST MODE 1 ENABLE	TEST MODE 1 DISABLE
16	24M_48M_SEL	DTRA#	48MHz	24MHz
15	2E_4E_SEL	RTSA#	4E	2E

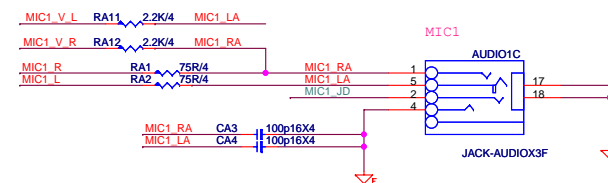
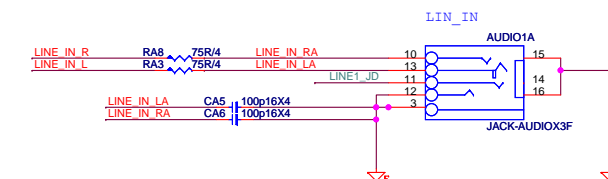
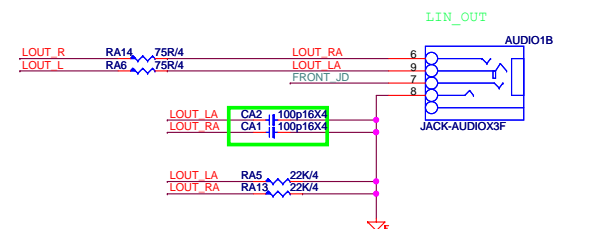
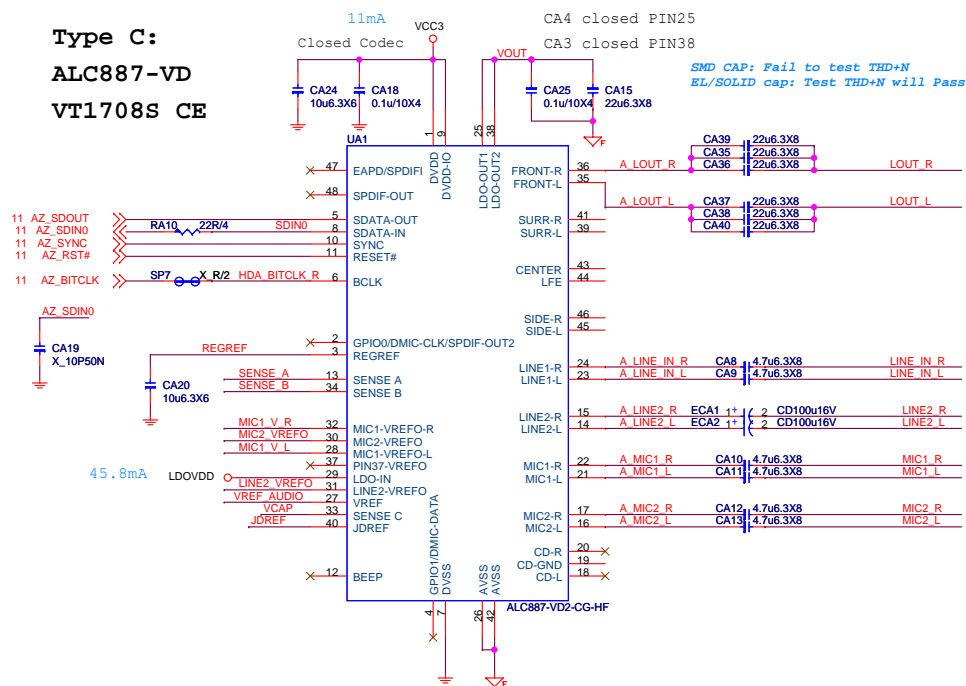
Voltage Sensing



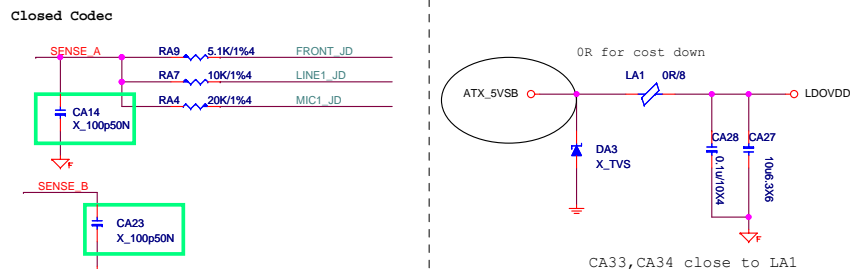
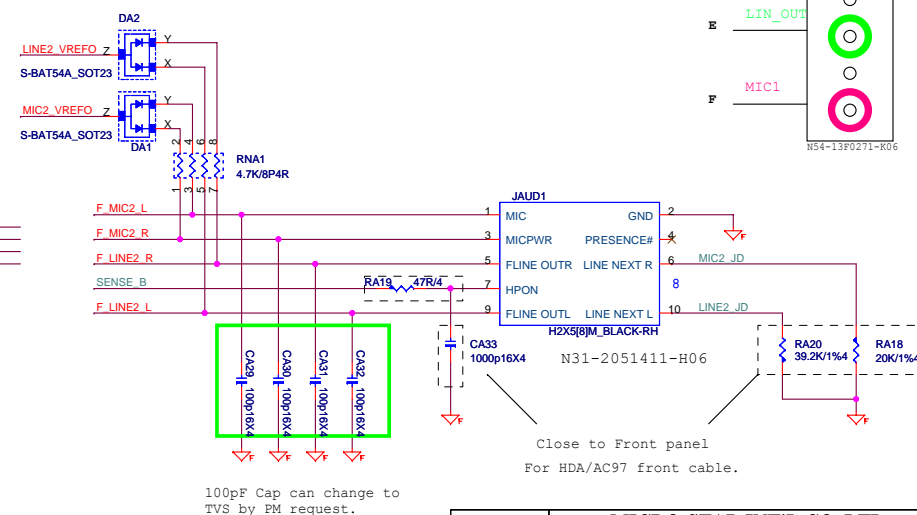
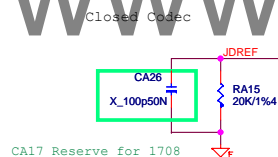
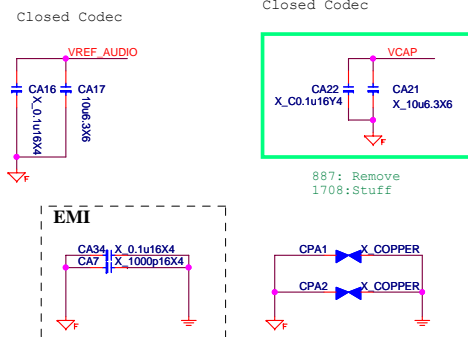
Thermal Resistor




Type C:
ALC887-VD
VT1708S CE

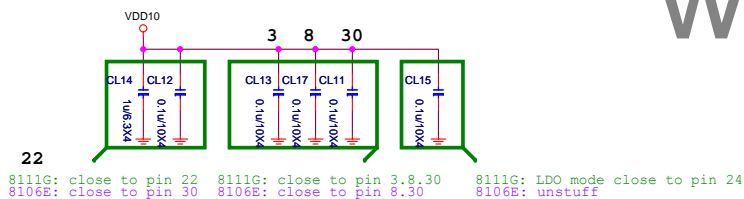
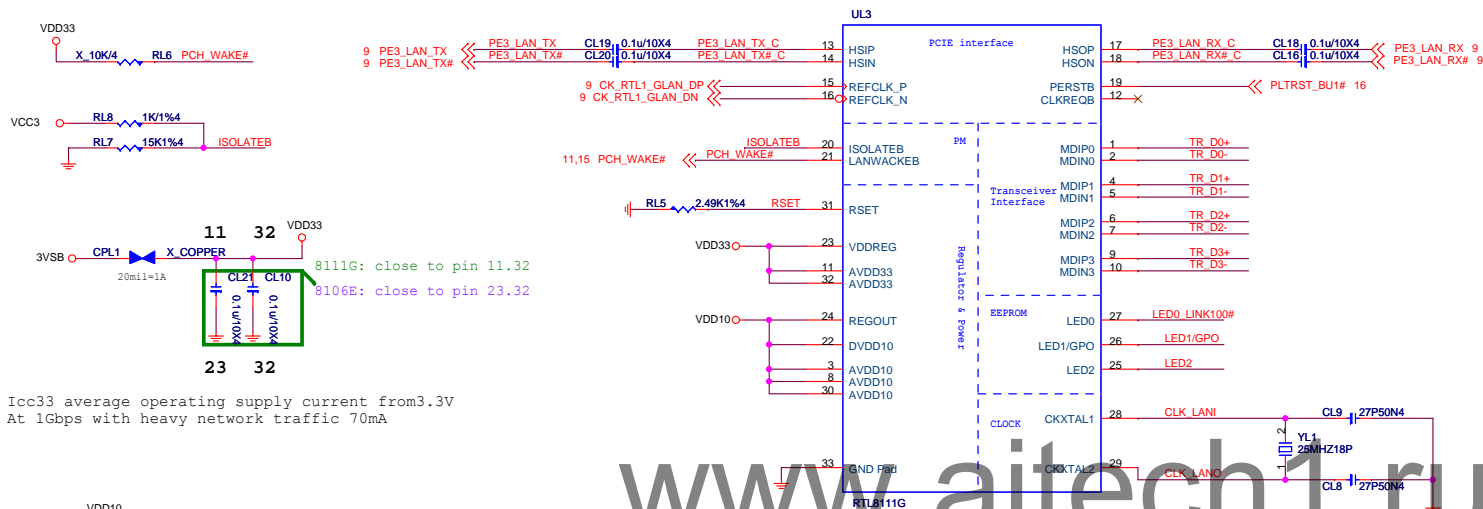


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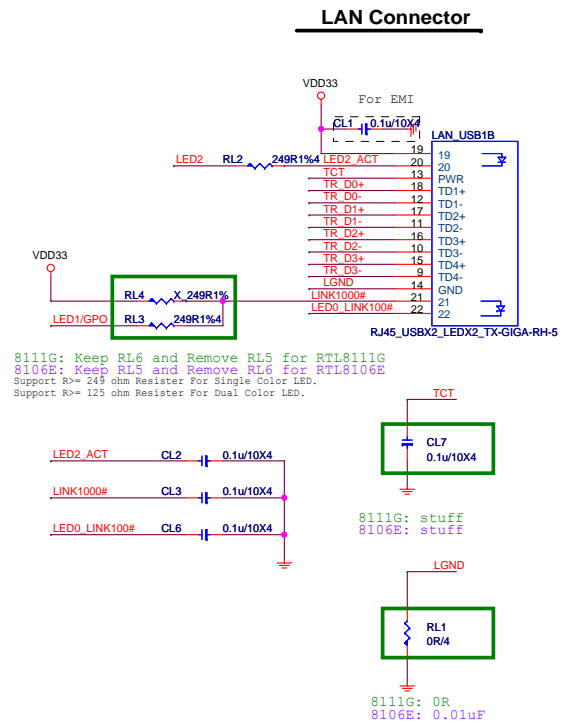


	MICRO-STAR INT'L CO.,LTD		
	MS-7817		
	Size Custom	Document Description Audio Codec ALC892/887	Rev 10
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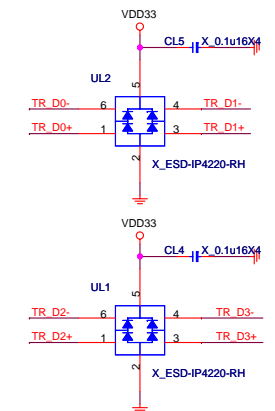
RTL8111G Giga LAN
RTL8106E 10/100M LAN



Icc10 average operating supply current from 1.0V
At 1Gbps with heavy network traffic 300mA



Reserve ESD Protect

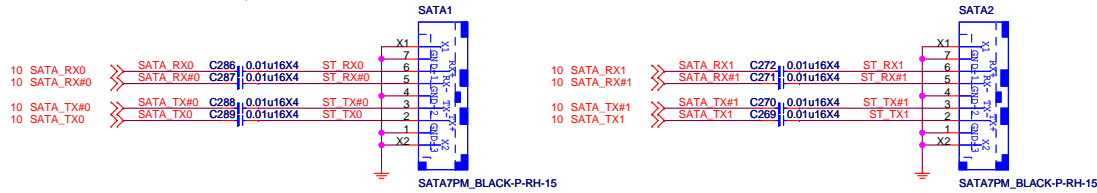


MICRO-STAR INT'L CO.,LTD

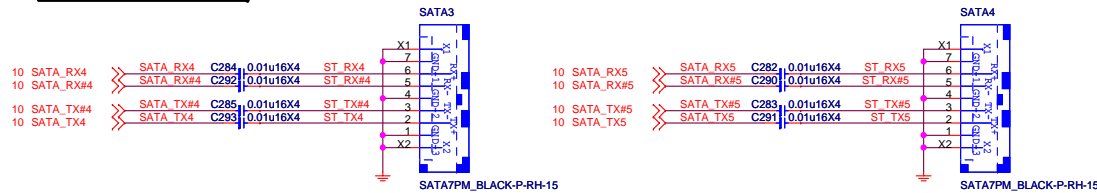
MS-7817

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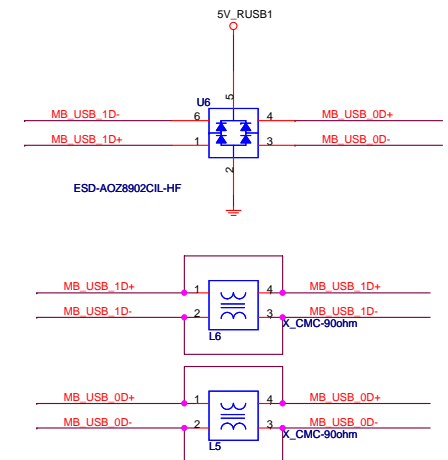
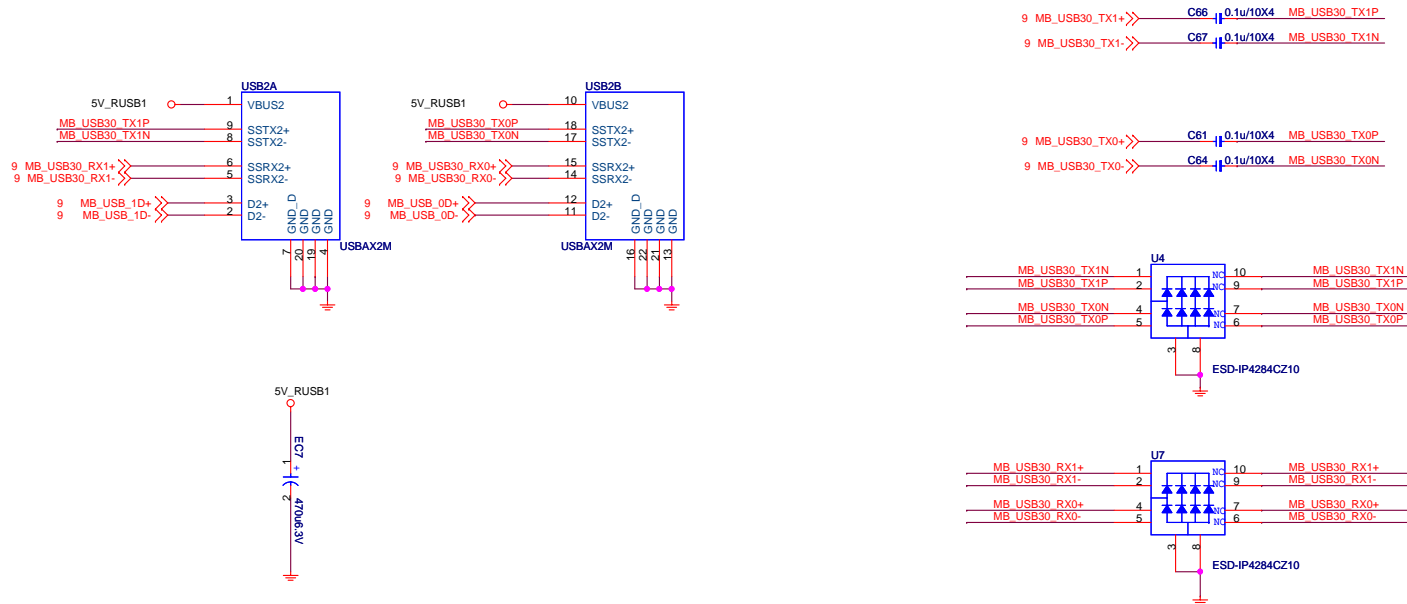
SATA 6G PORT 0,1



SATA 3G PORT 4,5



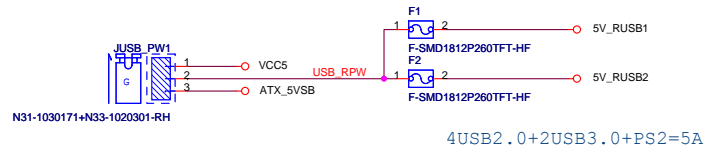
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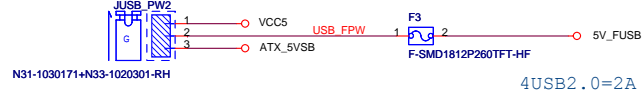
Type C: jumper +Fuse

PCH/FCH side: OC# pull high to +3VSB

Near Rear ==>



Near Front ==>

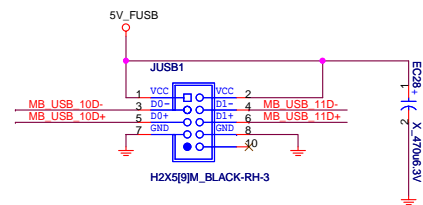
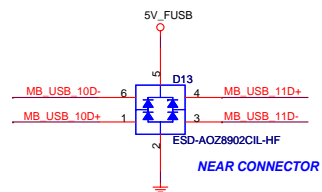
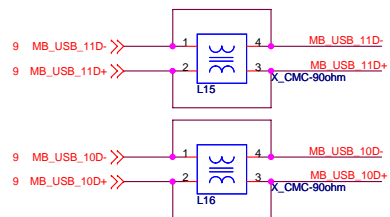


Default VCC5 (PIN1-2)

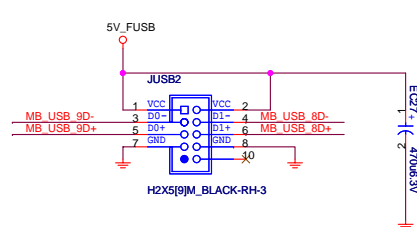
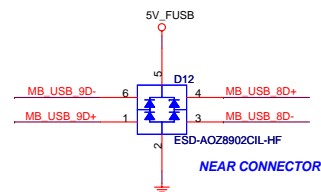
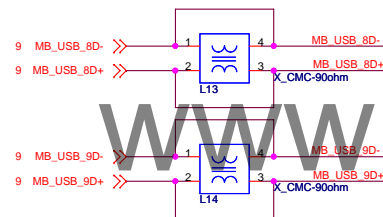
JUSB_FW	BIOS Menu	Wake up support
1-2	EUP Enable	Not support
	EUP Disable	Not support
2-3	EUP Enable	Not support
	EUP Disable	support

D08-2000300-P16 (Itrip=3.5A; 0.003ohm) support 6 USB ports (3A)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm) support 4 USB ports (2A)
D08-0100110-P16 (Itrip=1.1A; 0.04ohm) support 2 usb 2.0 ports (1A)

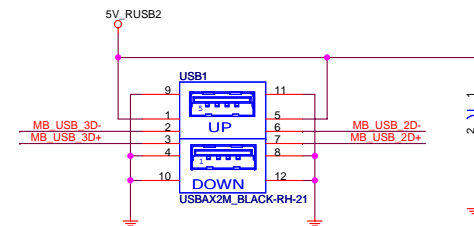
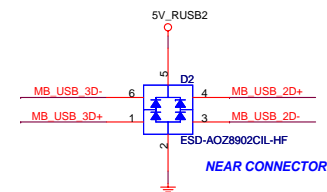
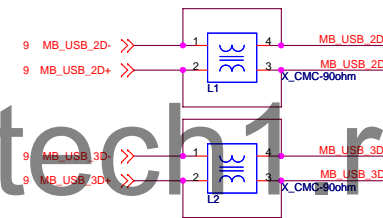
FRONT USB PORT 8,9



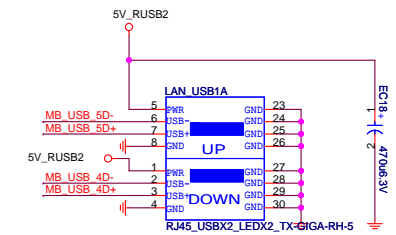
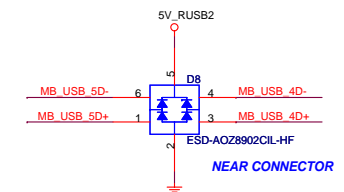
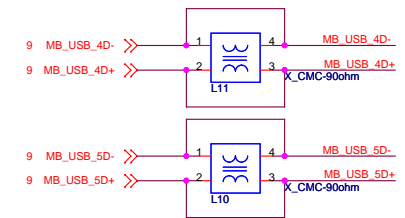
FRONT USB PORT 10,11



FRONT USB PORT 10,11



FRONT USB PORT 10,11



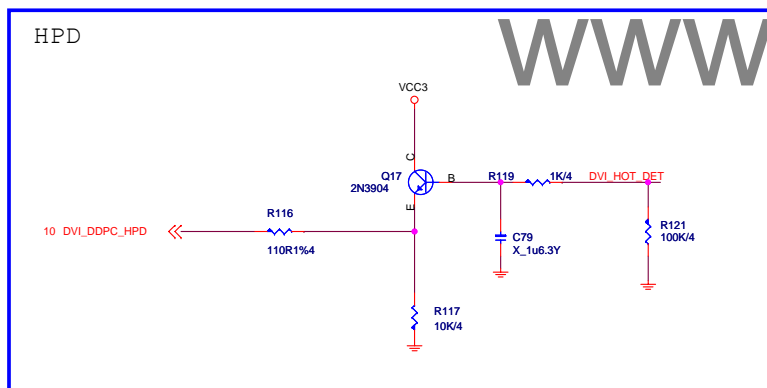
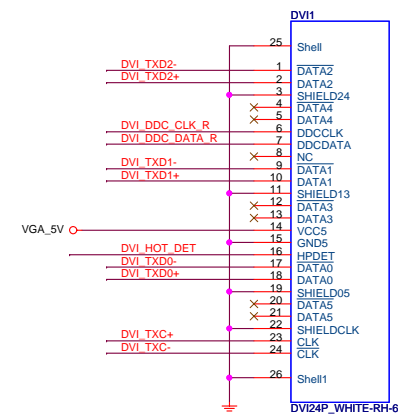
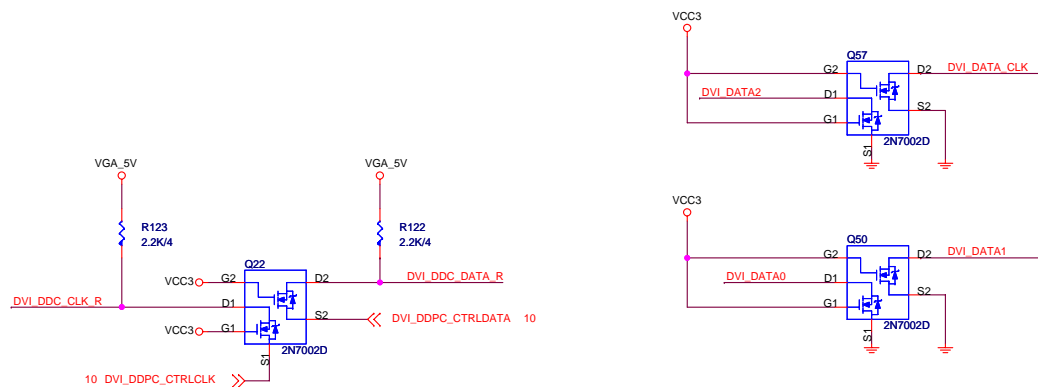
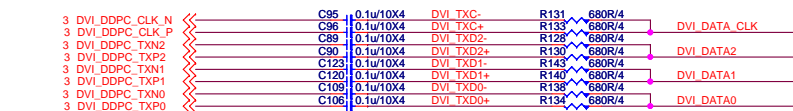
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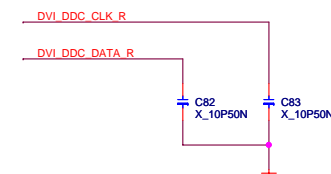
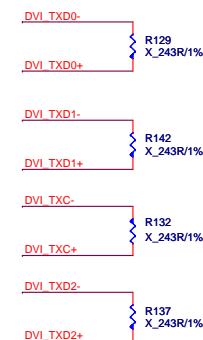
DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

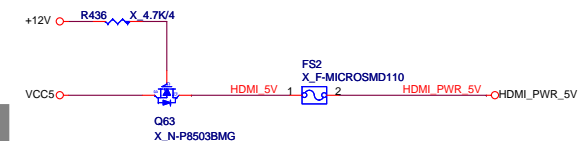
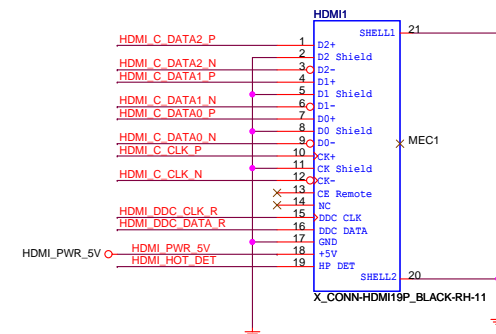
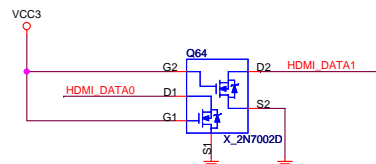
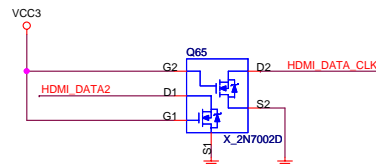
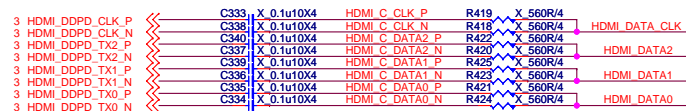


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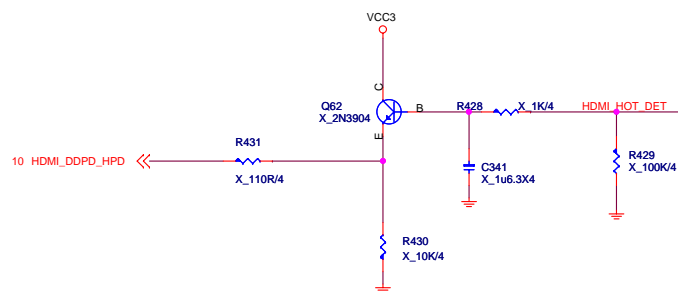
For EMI



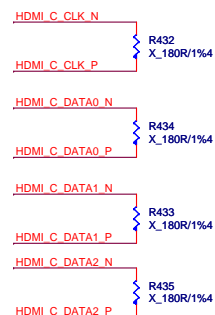
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



HPD



For EMI



EMI



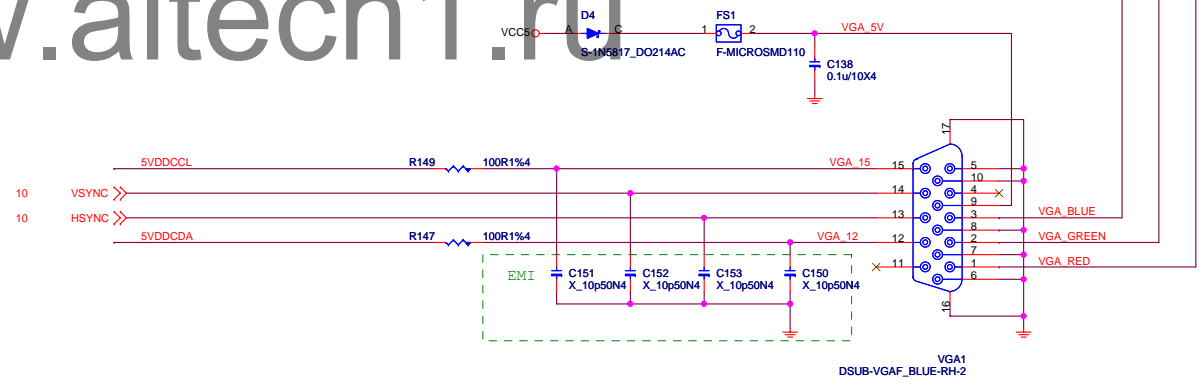
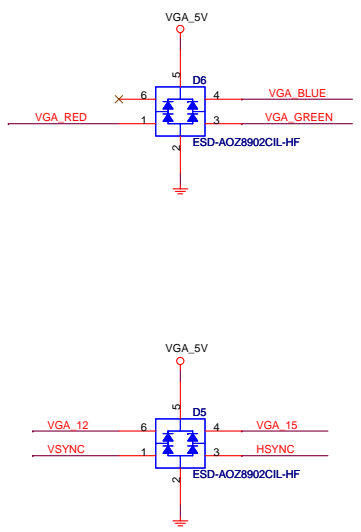
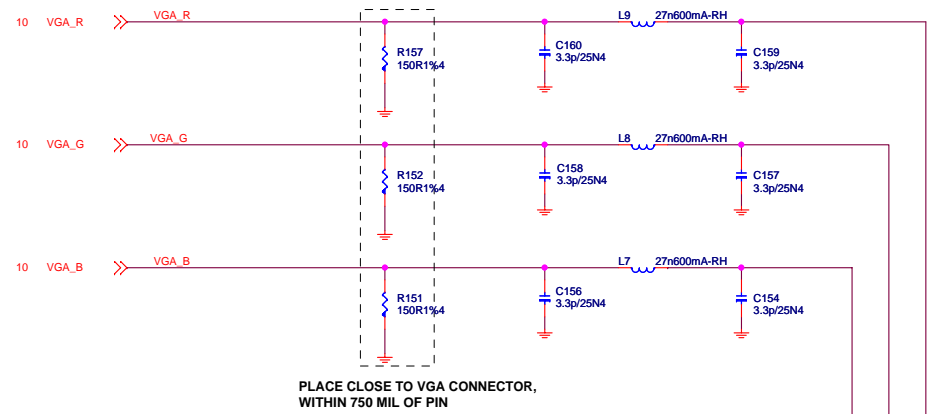
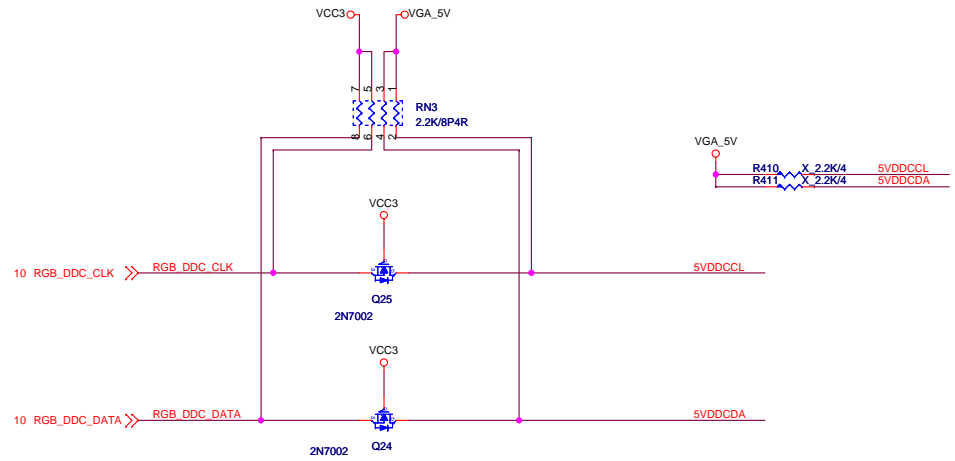
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Date: Wednesday, December 05, 2012	Sheet 22 of 36	

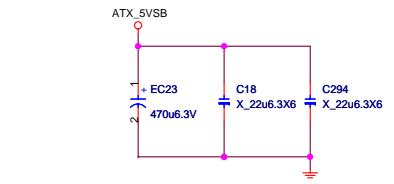
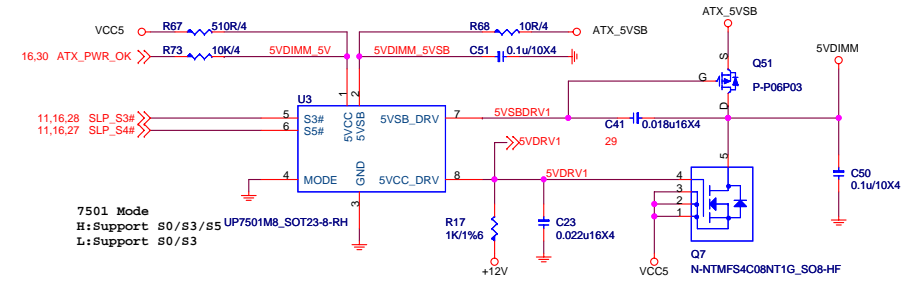
D-Sub

Level shift

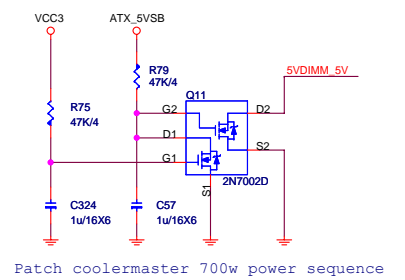


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5VDIMM FOR DDR

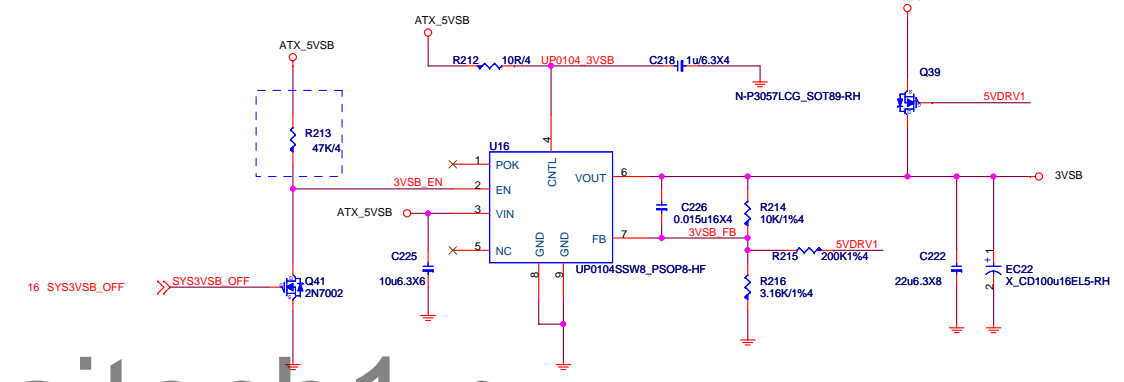


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



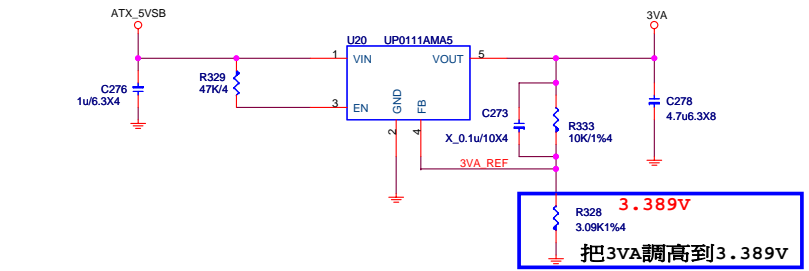
3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



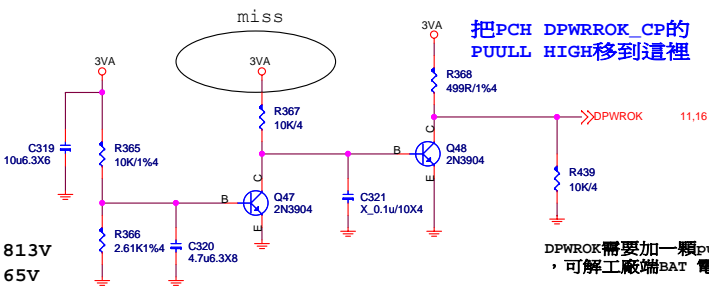
3VA

20mA



3.389V分壓=0.813V
2.71V分壓=0.65V

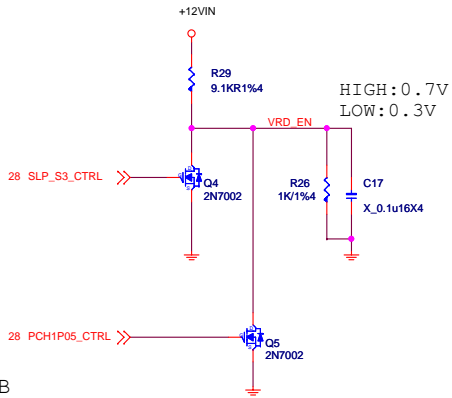
FOR DPWRK跟3VA的POWER
DOWN的時序(S5-->G3)



DPWRK需要加一顆pull down 10k電阻
，可解工廠端BAT 電流過大問題

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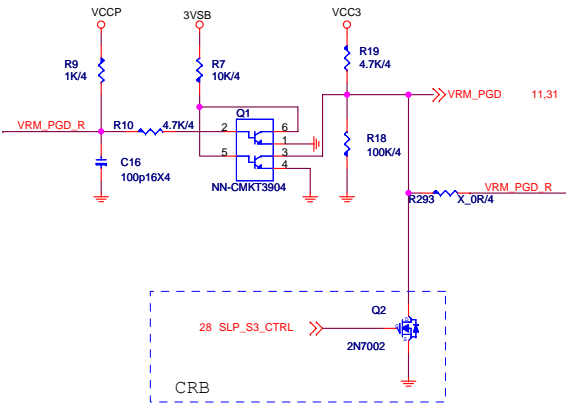
VCORE power on by s3 and 12v



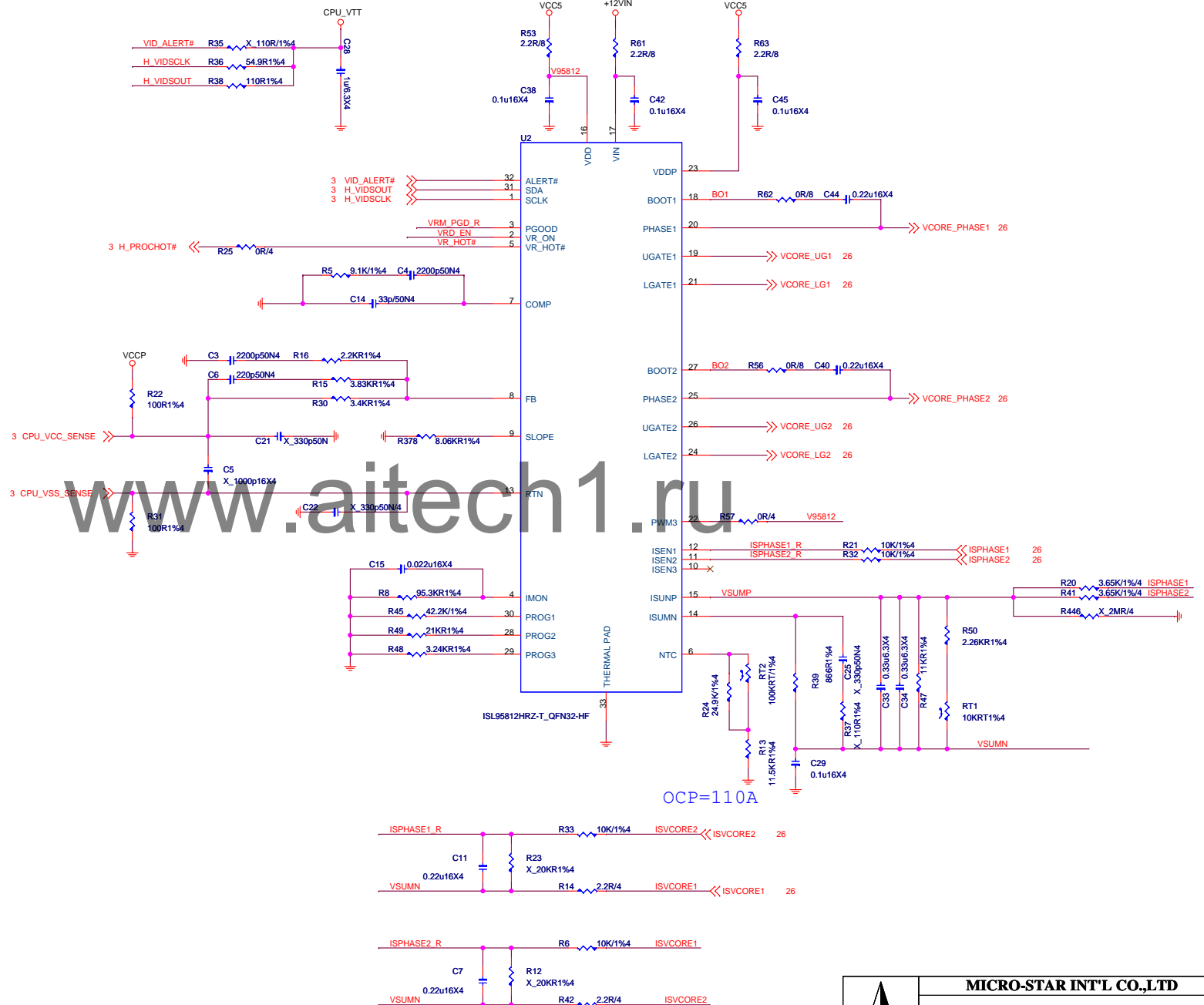
CRB

HIGH:by PCH_1P05V
LOW:by S3

VRMPWRGD LEVEL SHIFT



CRB



OCP=110A



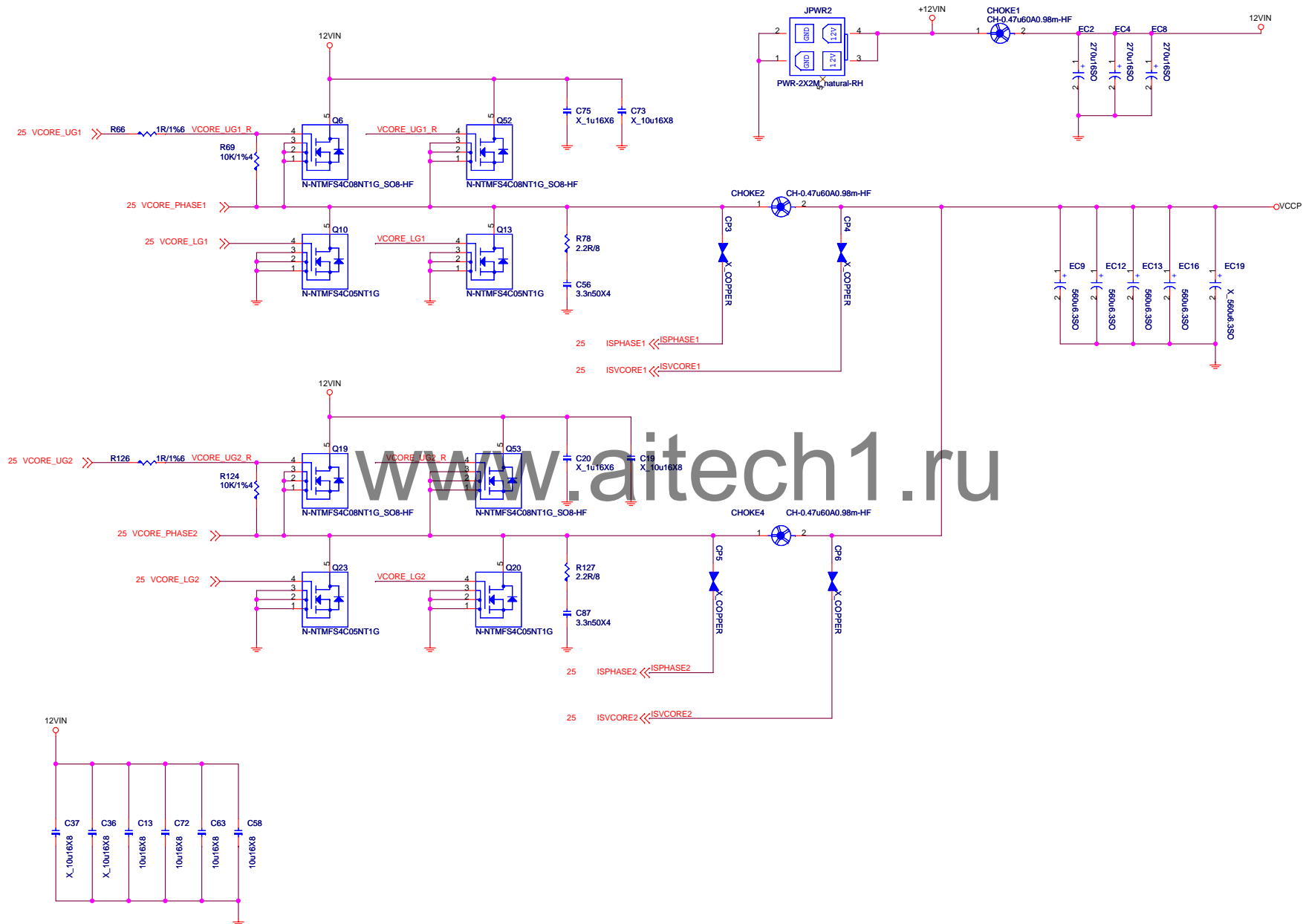
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VCCP POWER

VCORE ICC MAX70A ICCTDC:47A 65W
LL:2.5m ohm



DDR Power:1.5V

DDR3_1.5V 4.2A+6A+0.5A+7.661=18.361A OCP:66.7A

4.2A FOR CPU

6A FOR 2DIMM

0.5A FOR DDR VTT

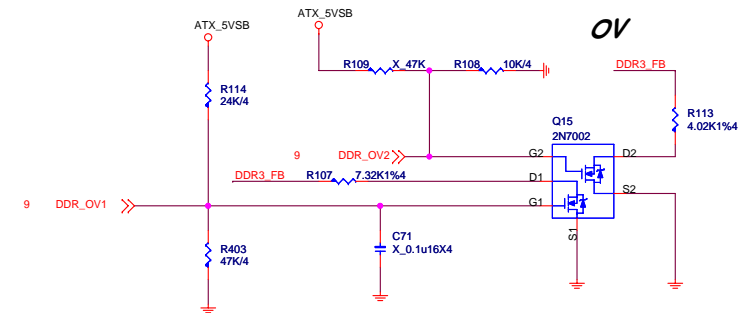
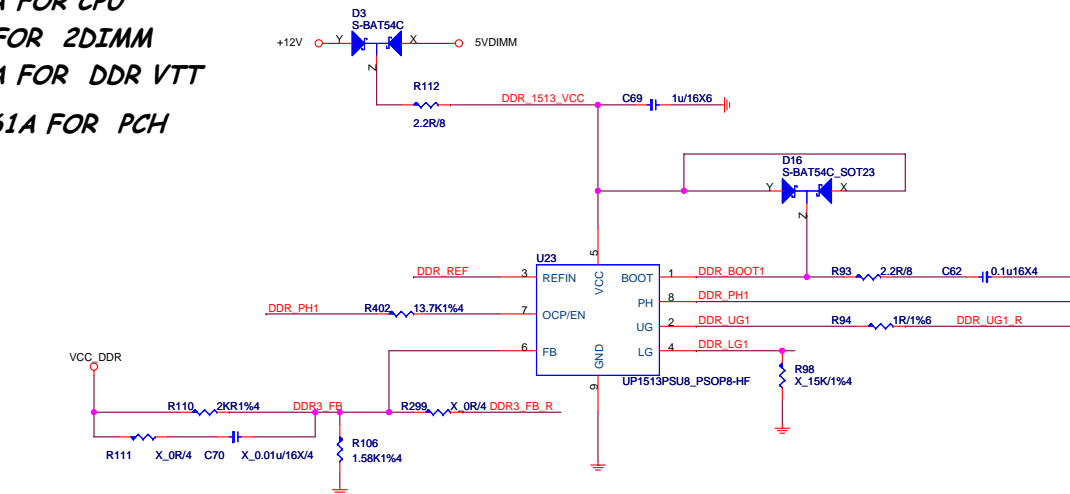
7.661A FOR PCH

$$OCP:16.447*1.5=24.6705A$$

$$OCPXRdson(Low\ side)=(40uA*Rocs(R122)-0.4V)$$

$$Rocs(R122)=13.75K$$

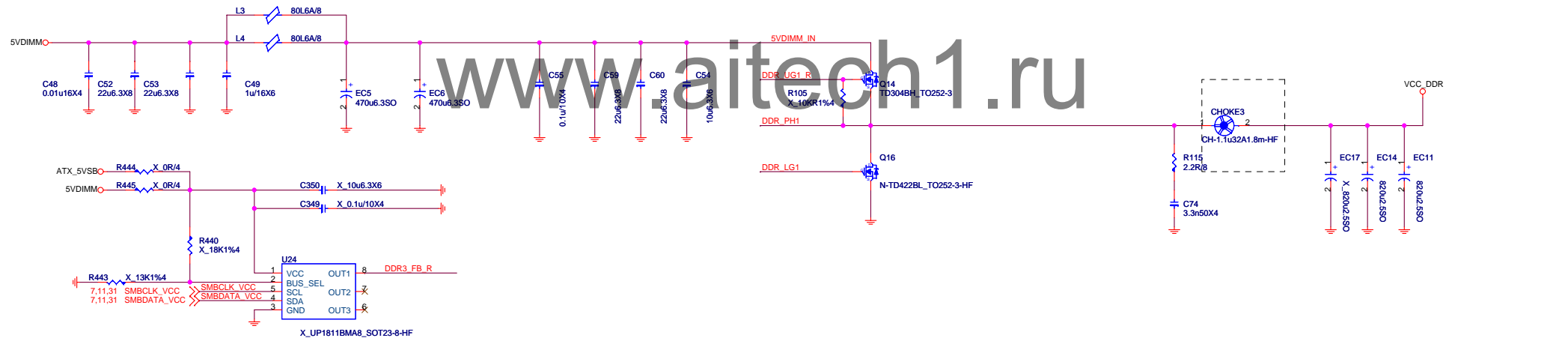
2012.03.22 Modify Pull hi (47K) to ATX_5VSB



*Default 1.5V

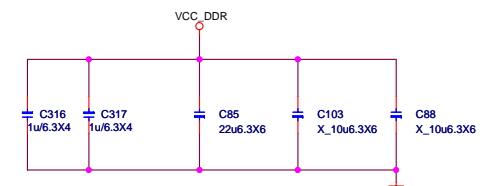
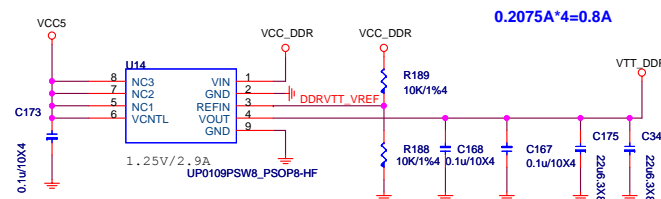
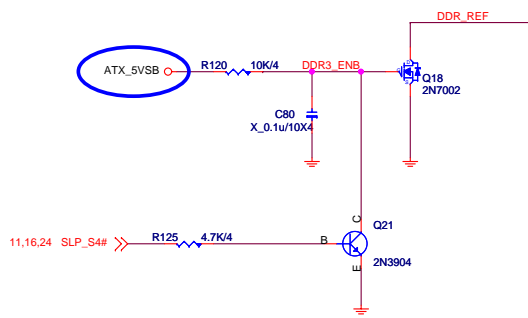
DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01 (S/IO)
DDR_OV2 = GPIO02 (S/IO)



DDR VTT Power

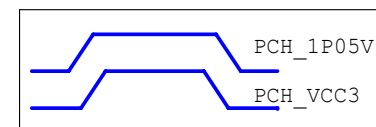
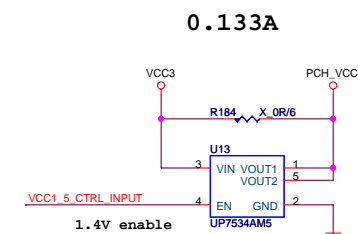
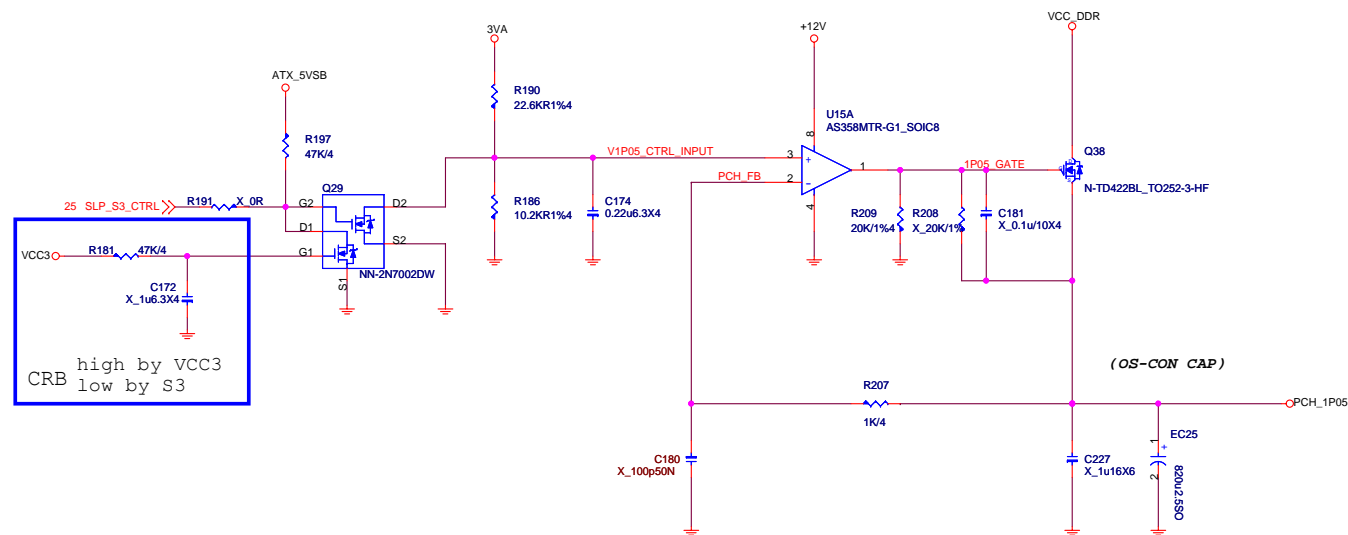
To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



MSI			
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Size	Document Description	Rev	
Custom	DDR Power - UP6103 1-Phase	10	
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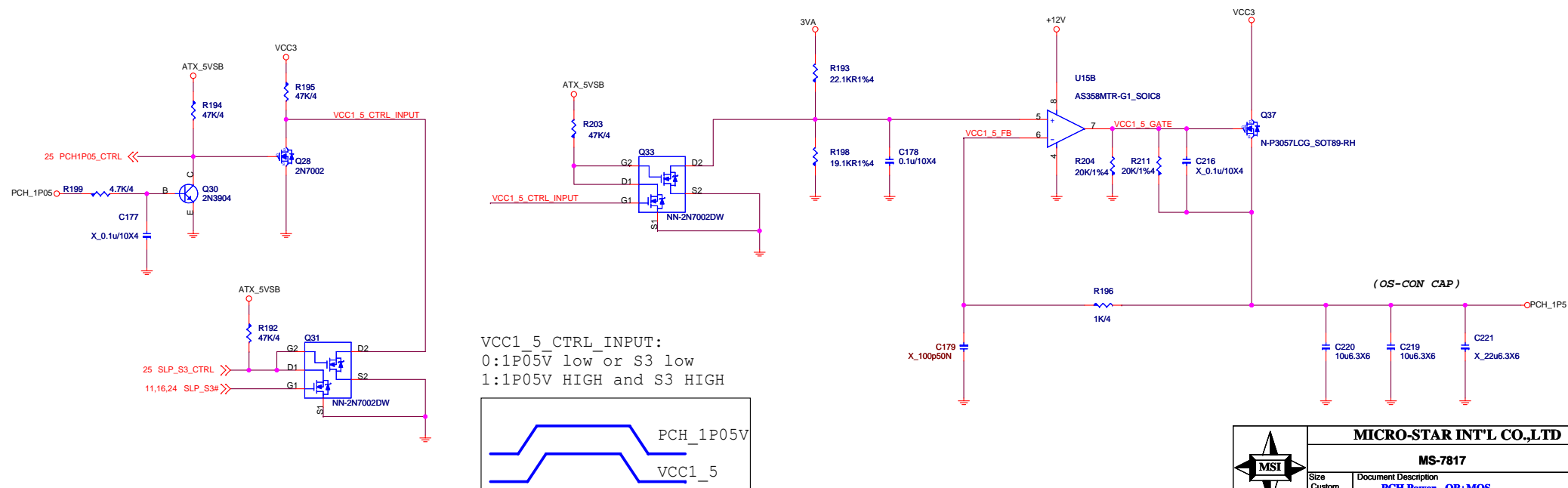
P.S. Only for meet Intel power down sequence.

PCH Power:1.05V 5.747A



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PCH Power:1.5V 0.183A

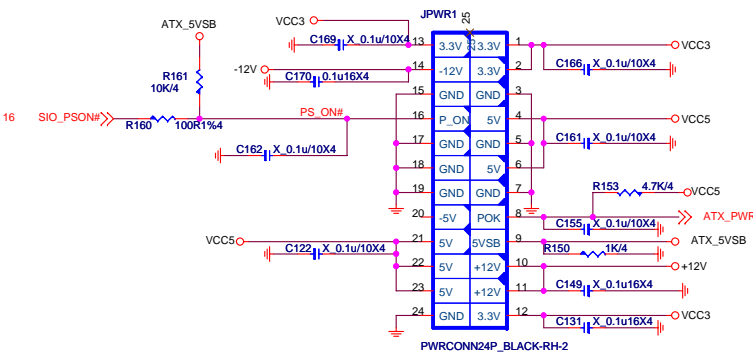


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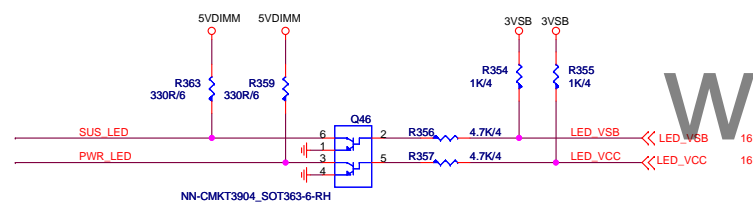
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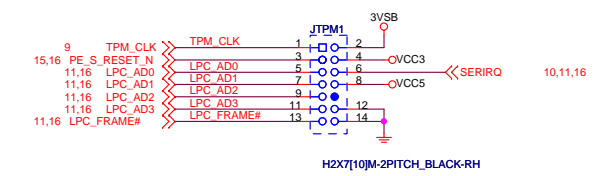
ATX POWER CONNECTOR



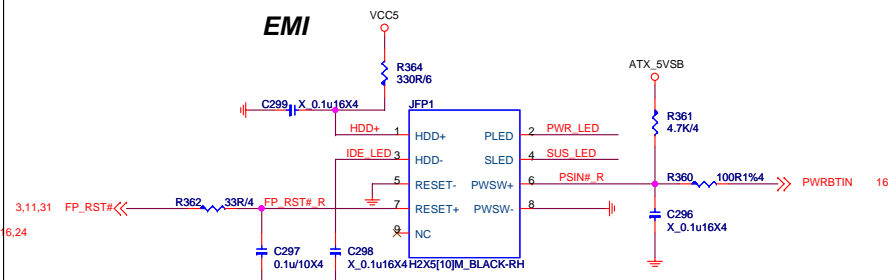
LED (for NV5533)



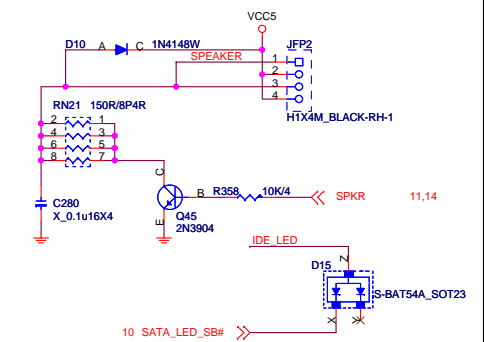
TPM/JLPC



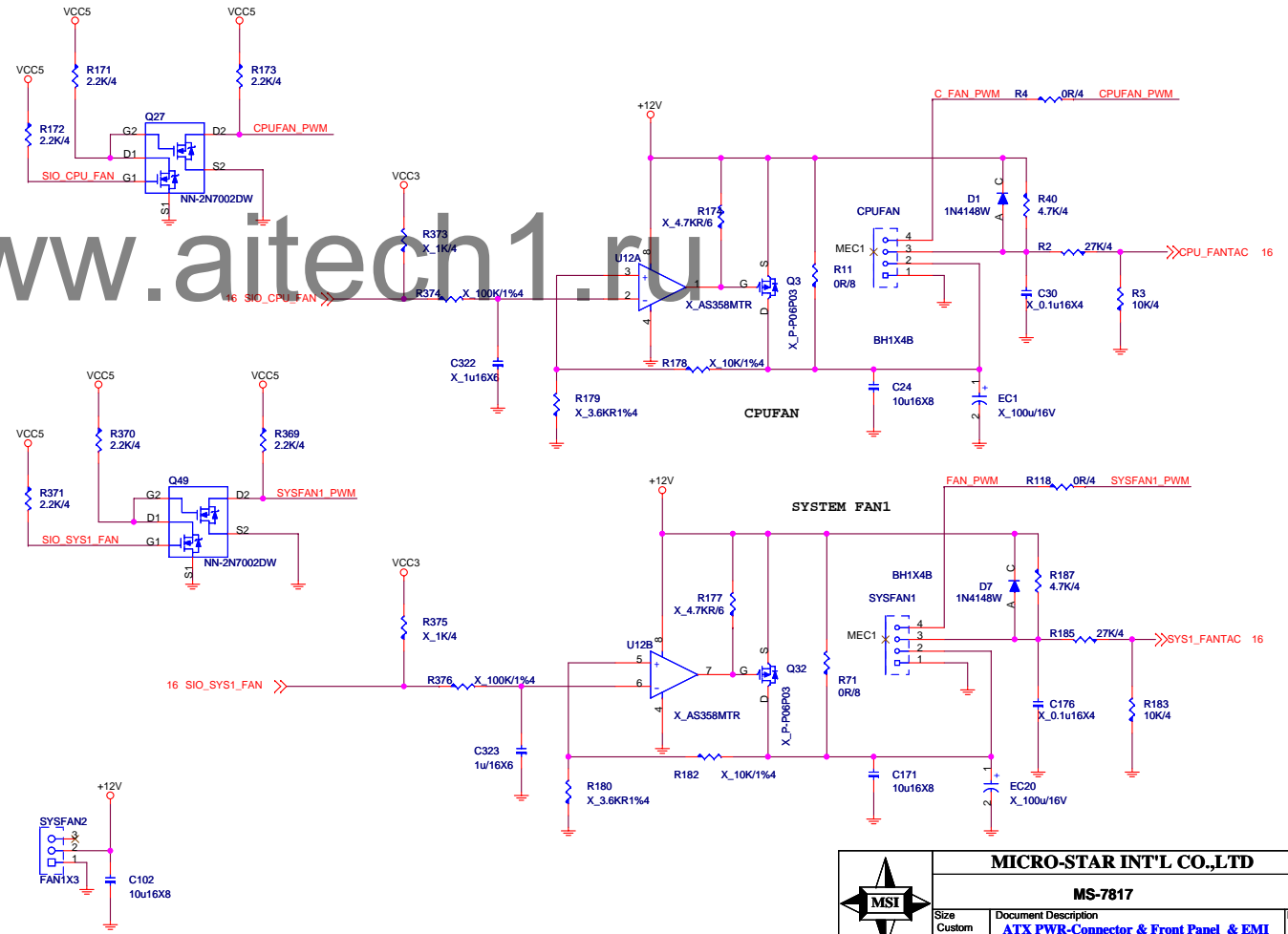
FRONT PANNEL



Speaker Pin Header



FAN-COUNTROL CIRCUIT

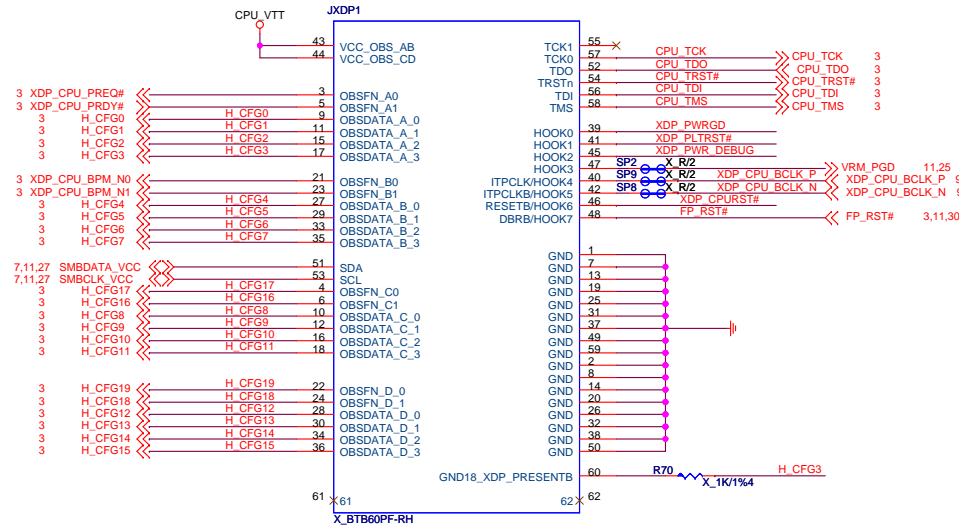


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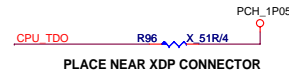
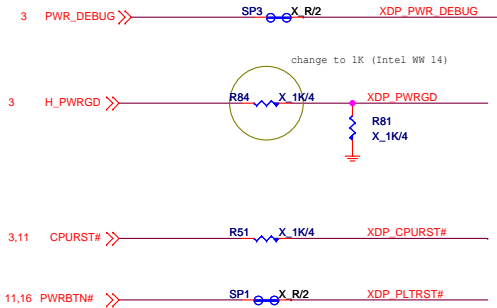
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Reserve debug port 5020

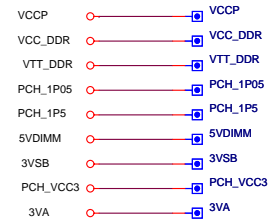
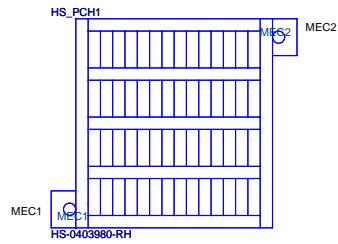


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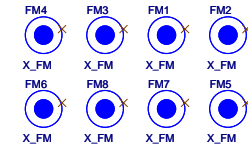




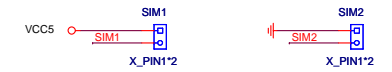
PCH XDP PWRGD/RESET



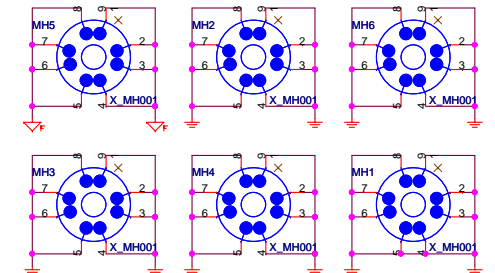
Optical Fiducial Marks-120



Simulation



Mounting Holes



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